

DJ1 Calpella UMA Schematics Document

Arrandale

Intel PCH

2010-04-23

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REV: X01

DY : Nopop Component

<Core Design>



Wistron Corporation
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Title

Cover Page

Size
A3

Document Number

DJ1 Calpella UMA

Rev

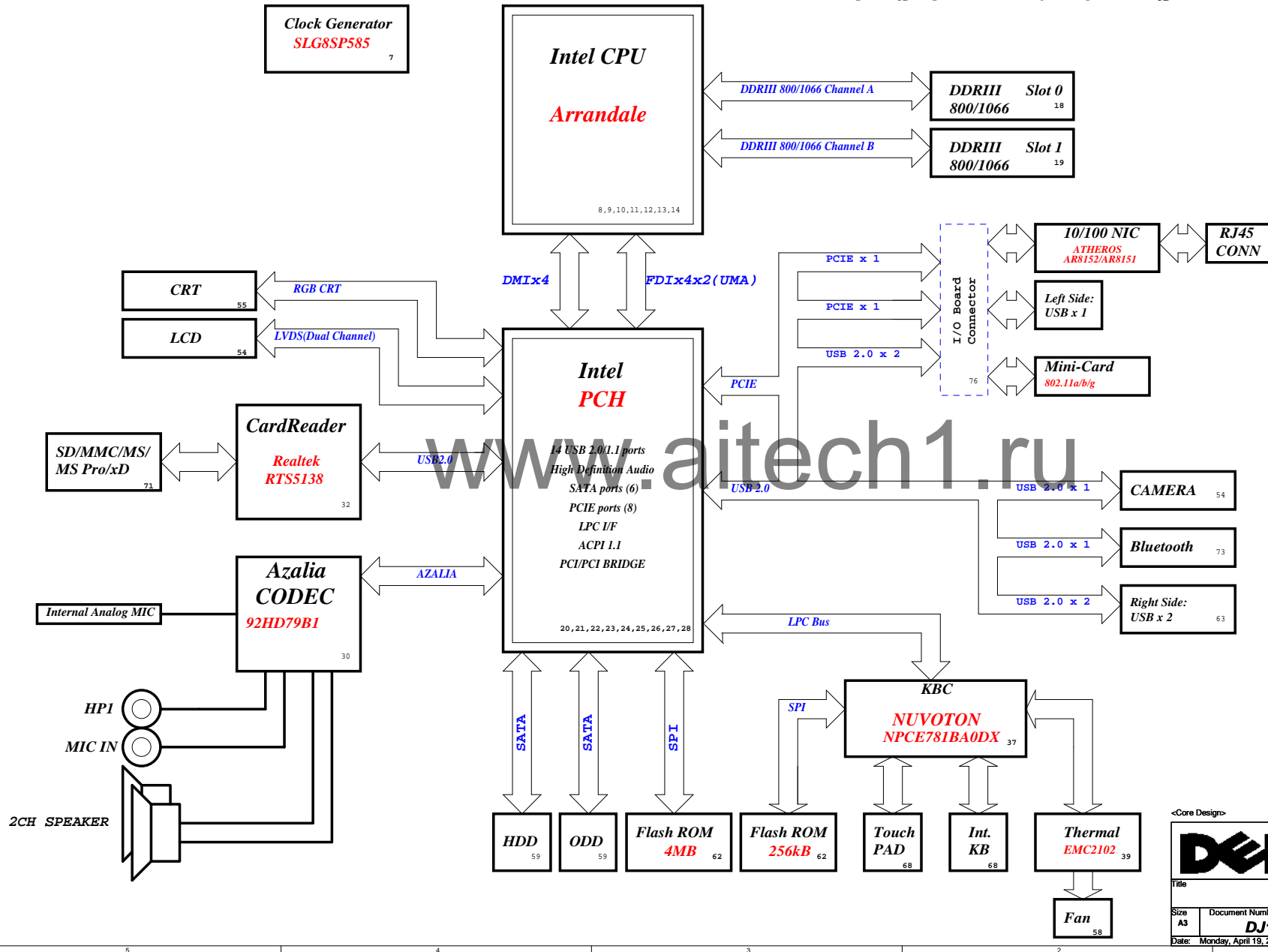
X01

Date: Monday, April 26, 2010

Sheet 1 of 90

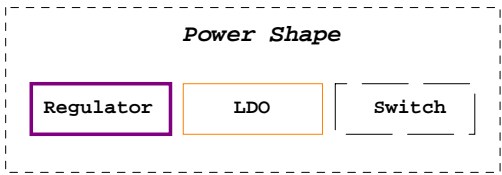
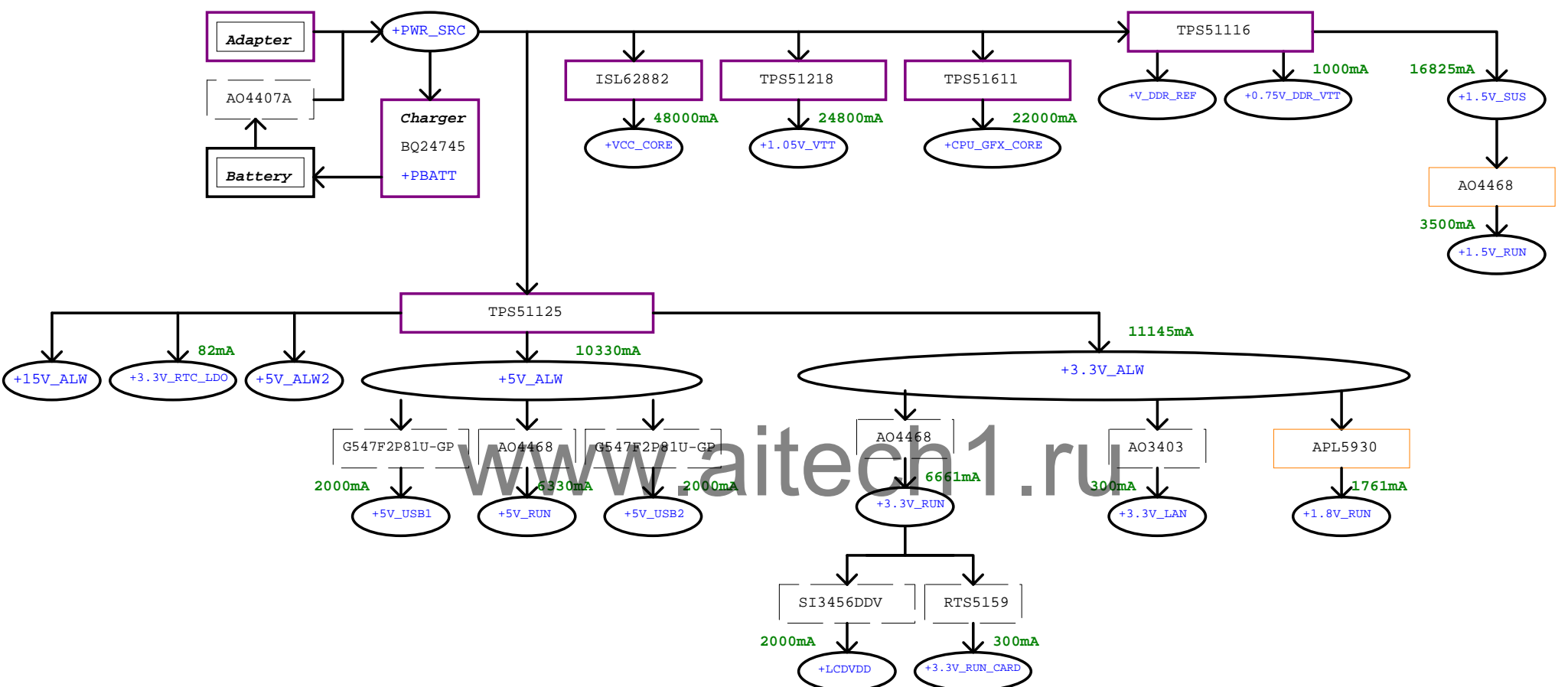
DJ1 UMA Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK19.0SB
Revision : 10212-SB

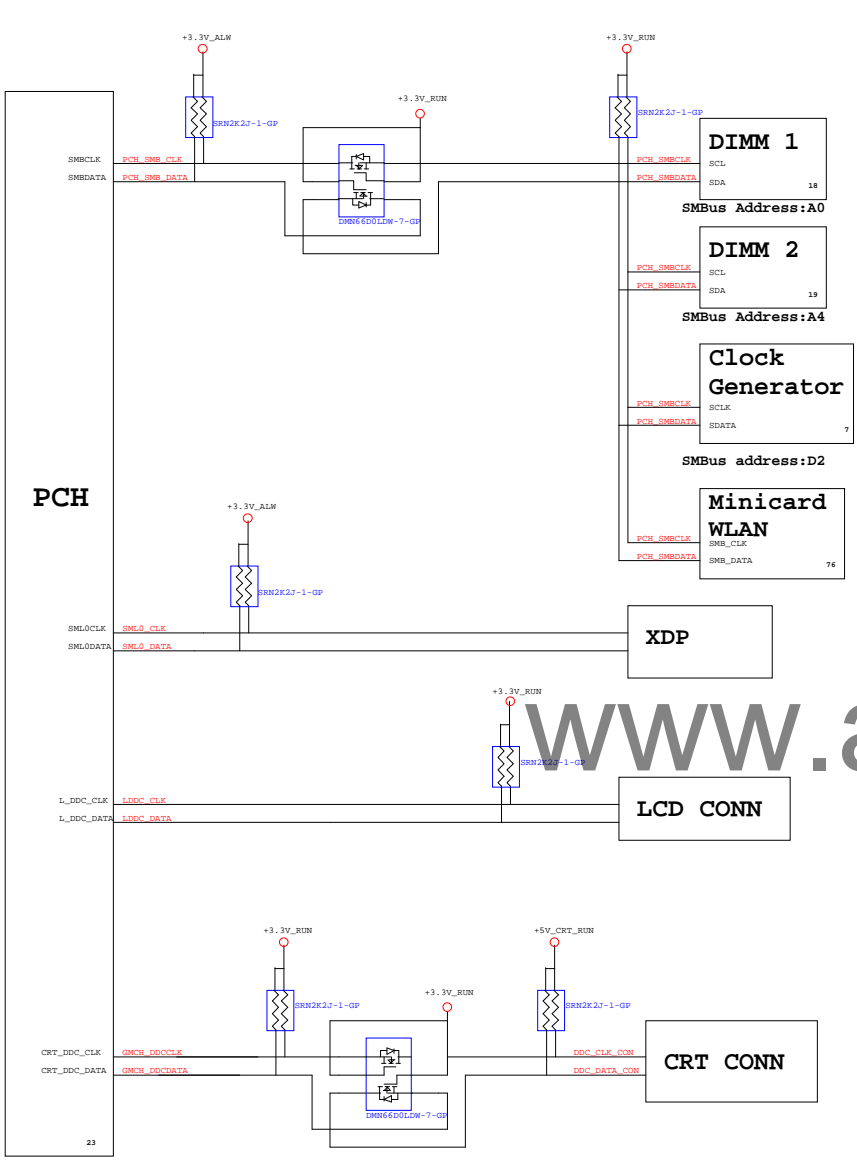


CPU DC/DC	
ISL62882 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC	
TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC	
RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC	
RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC	
TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE
MAXIM CHARGER	
BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC	
APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
SYSTEM DC/DC	
Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

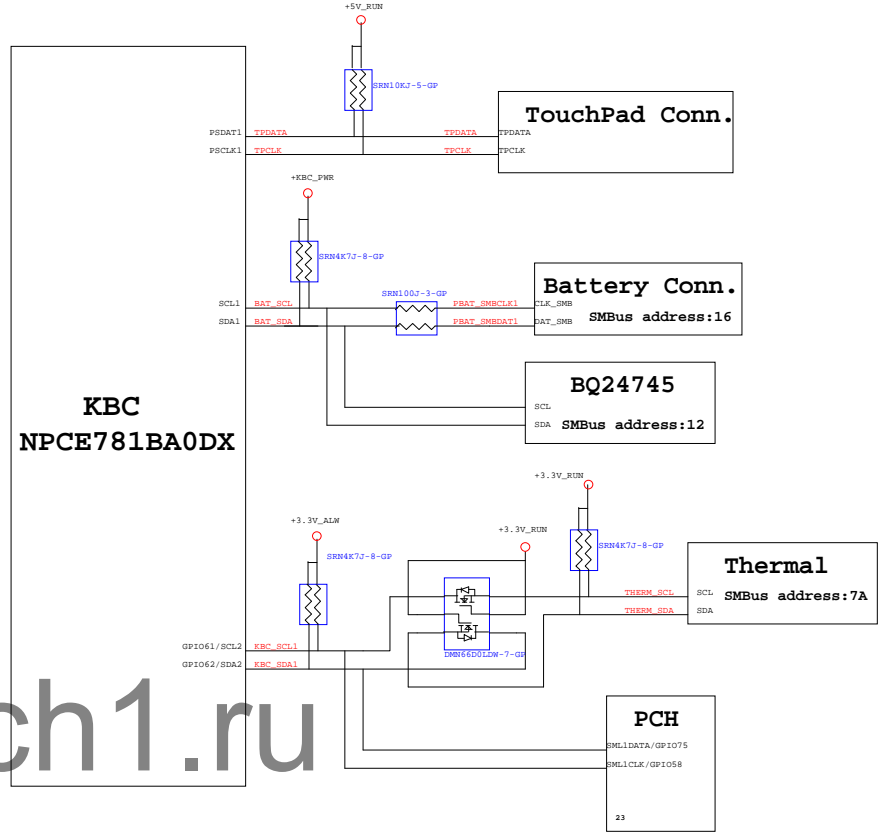
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Title Block Diagram		
Size A3	Document Number DJ1 Calpella UMA	Rev X01
Date: Monday, April 19, 2010	Sheet 2	of 90



PCH SMBus Block Diagram

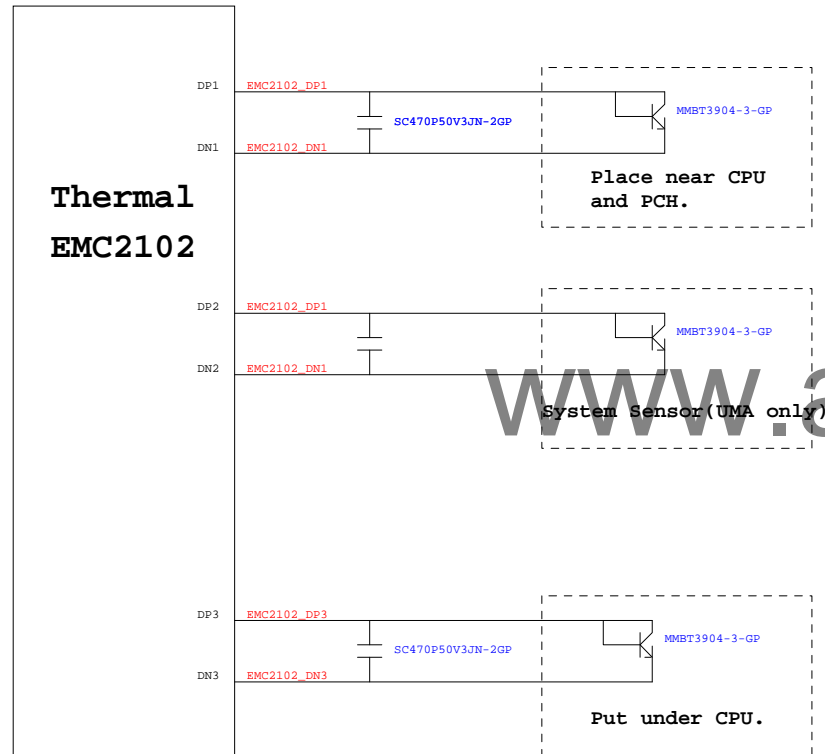


KBC SMBus Block Diagram

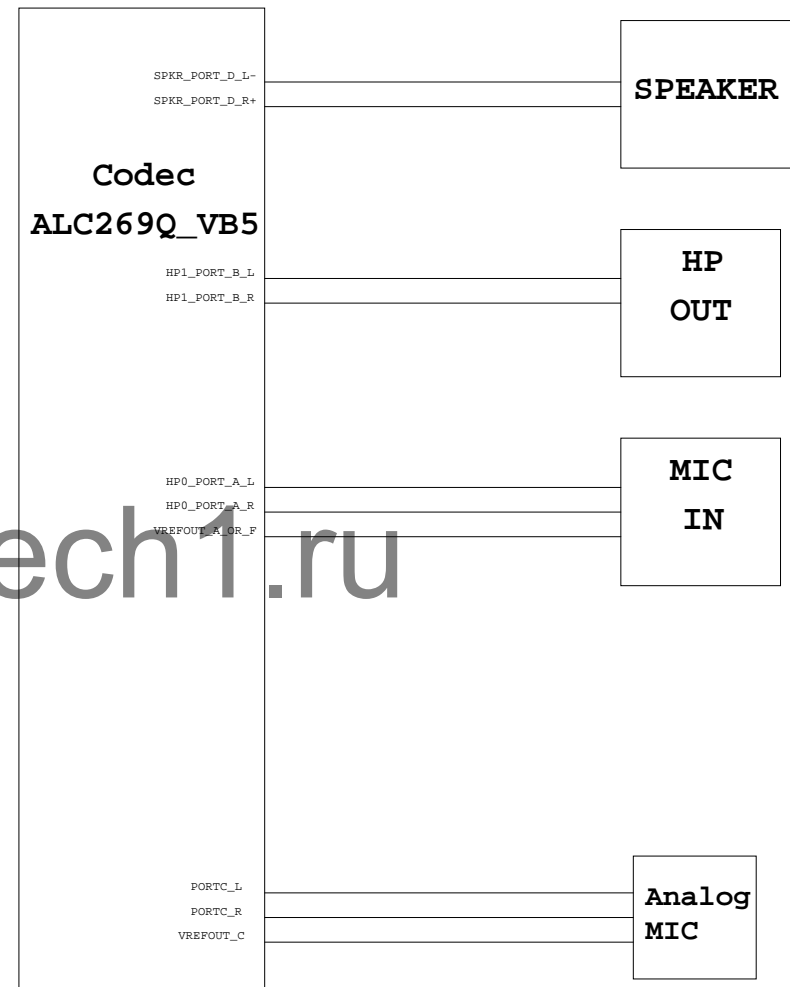


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Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-k- 10-k weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-k weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-k pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-k pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-k pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-k weak pull- up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-k weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-k weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

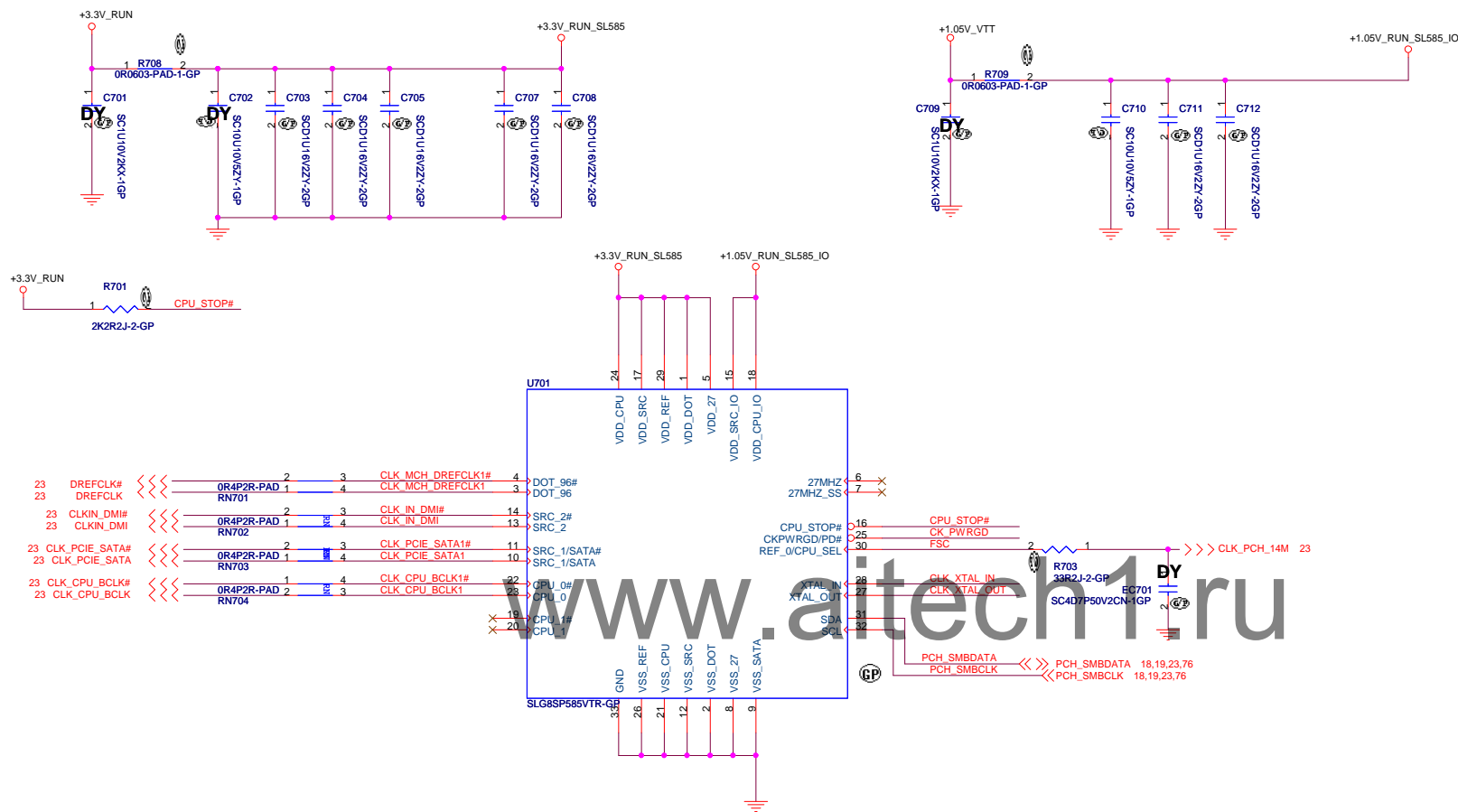
Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

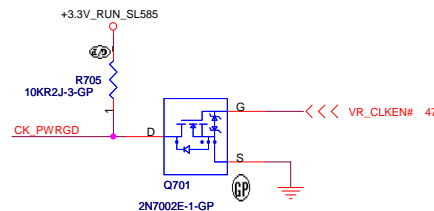
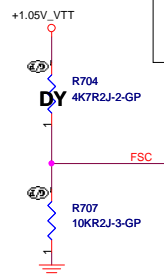
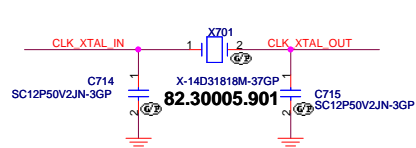
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Title			
<i>Table of Content</i>			
Size A3	Document Number DJ1 Calpella UMA	Rev X01	
Date: Friday, April 16, 2010	Sheet 6	of	90

SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz



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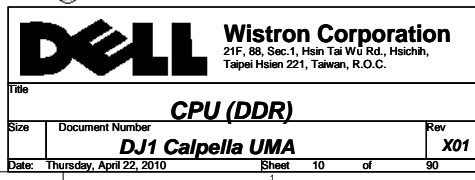
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Clock Generator SLG8SP585

Size Document Number Rev
DJ1 Calpella UMA X01

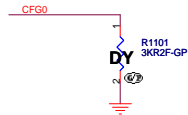
Date: Thursday, April 22, 2010 Sheet 7 of 90

Date: Thursday, April 22, 2010 Sheet 8 of 90

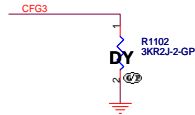
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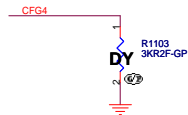
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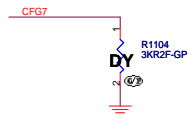
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



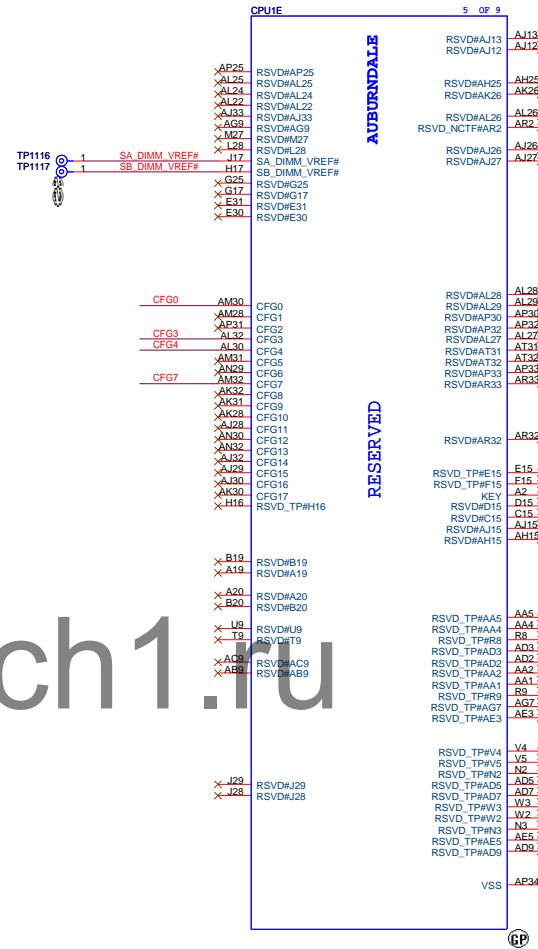
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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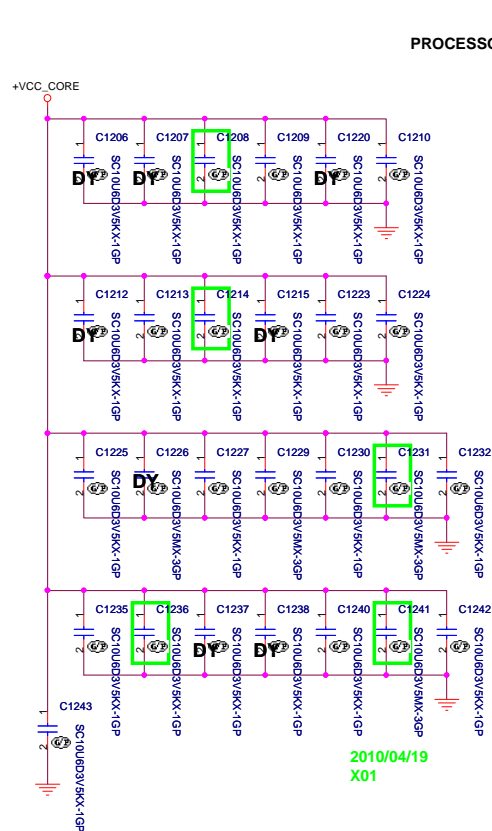


Title	
CPU (RESERVED)	
Size	Document Number
	DJ1 Calpella UMA
Date: Friday, April 16, 2010	Sheet 11 of 90

Rev

X01

SSID = CPU



2010/04/19
X01

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

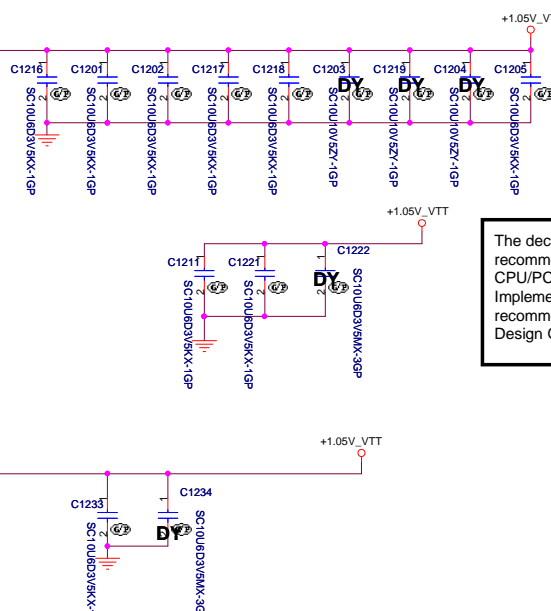
AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AF26 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AD26 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
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AC27 VCC
AC26 VCC
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Y14 VCC
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Y11 VCC
Y10 VCC
Y9 VCC
Y8 VCC
Y7 VCC
Y6 VCC
Y5 VCC
Y4 VCC
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V25 VCC
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V23 VCC
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V21 VCC
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V19 VCC
V18 VCC
V17 VCC
V16 VCC
V15 VCC
V14 VCC
V13 VCC
V12 VCC
V11 VCC
V10 VCC
V9 VCC
V8 VCC
V7 VCC
V6 VCC
V5 VCC
V4 VCC
V3 VCC
V2 VCC
V1 VCC
V0 VCC

VTT0 AH14
VTT0 AH12
VTT0 AH11
VTT0 AH10
VTT0 J14
VTT0 J13
VTT0 J12
VTT0 J11
VTT0 G14
VTT0 G13
VTT0 G12
VTT0 G11
VTT0 F14
VTT0 F13
VTT0 F12
VTT0 F11
VTT0 E14
VTT0 E13
VTT0 E12
VTT0 D13
VTT0 D12
VTT0 D11
VTT0 C14
VTT0 C13
VTT0 C12
VTT0 C11
VTT0 B14
VTT0 B12
VTT0 A14
VTT0 A13
VTT0 A12
VTT0 A11

VTT0 AF10
VTT0 AE10
VTT0 AC10
VTT0 AB10
VTT0 Y10
VTT0 W10
VTT0 U10
VTT0 T10
VTT0 J12
VTT0 J11
VTT0 J16
VTT0 J15

PSI# AN33 >>> PSI# 47
>>> H_VID[6..0] 47
AK35 H_VID0
AK33 H_VID1
AK34 H_VID2
AL35 H_VID3
AL33 H_VID4
AM33 H_VID5
AM35 H_VID6
AM34
PROC_DPRSPLVR >>> PM_DPRSPLVR 47
VTT_SELECT G15 H_VTTVID1 1 TP1201TPAD14-GP
H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

ISENSE AN35 <<< IMVP_IMON 47
VCC_SENSE A134 >>> VCC_SENSE 47
VSS_SENSE A135 >>> VSS_SENSE 47
VTT_SENSE B15 <<< TP_VSS_SENSE_VTT1 <<< VTT_SENSE 49
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT1 TP1202TPAD14-GP



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V

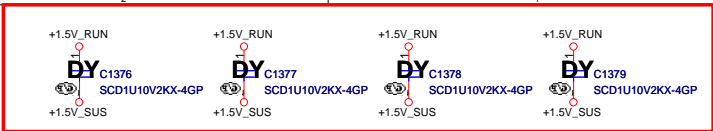
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CPU (VCC CORE)				
Size	Document Number			Rev
DJ1 Calpella UMA				
Date:	Thursday, April 22, 2010	Sheet	12 of	90

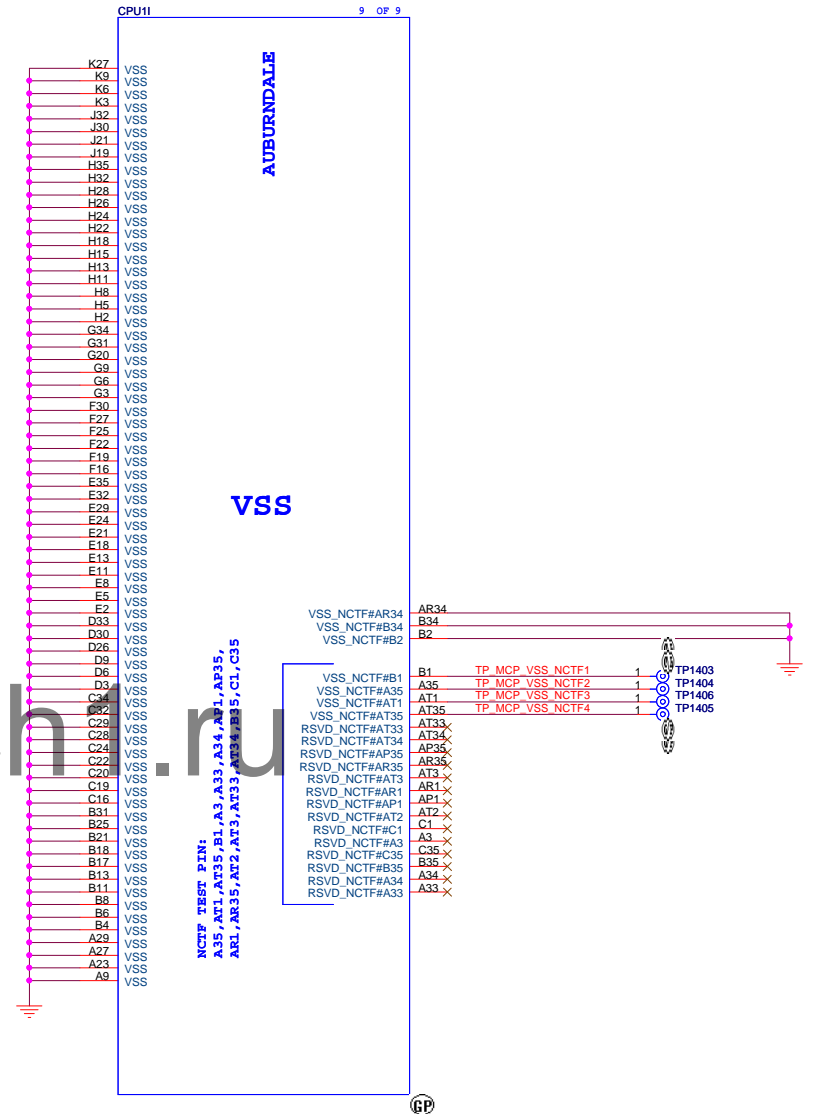
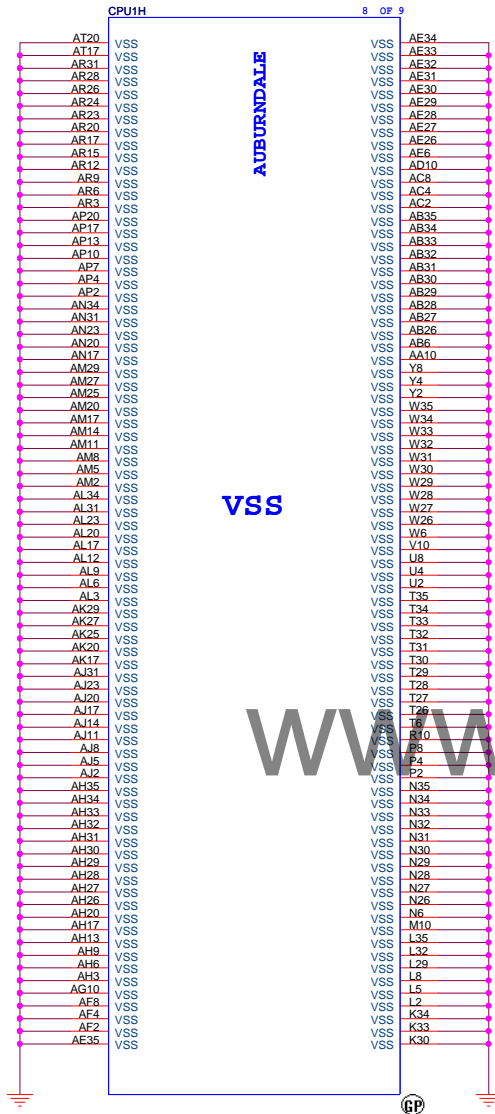
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Please note that the VTT Rail Values are: Auburndale VTT=1.05V
Clarksfield VTT=1.1V

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Title			
CPU (VCC GFXCORE)			
Size	Document Number		Rev
	DDJ Calpella UMA		X01
Date:	Thursday, 22, 2010	Sheet 13 of	90



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Reserved


Size A3	Document Number DJ1 Calpella UMA	Rev X01
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Date: Friday, April 16, 2010	Sheet 15 of 90
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Date: Friday, April 16, 2010	Sheet 1	16	of	90
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Size

A3

Document Number

DJ1 Calpella UMA

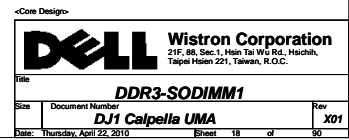
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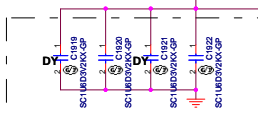
Date: Friday, April 16, 2010

Sheet 17 of 90

62.10017.P11

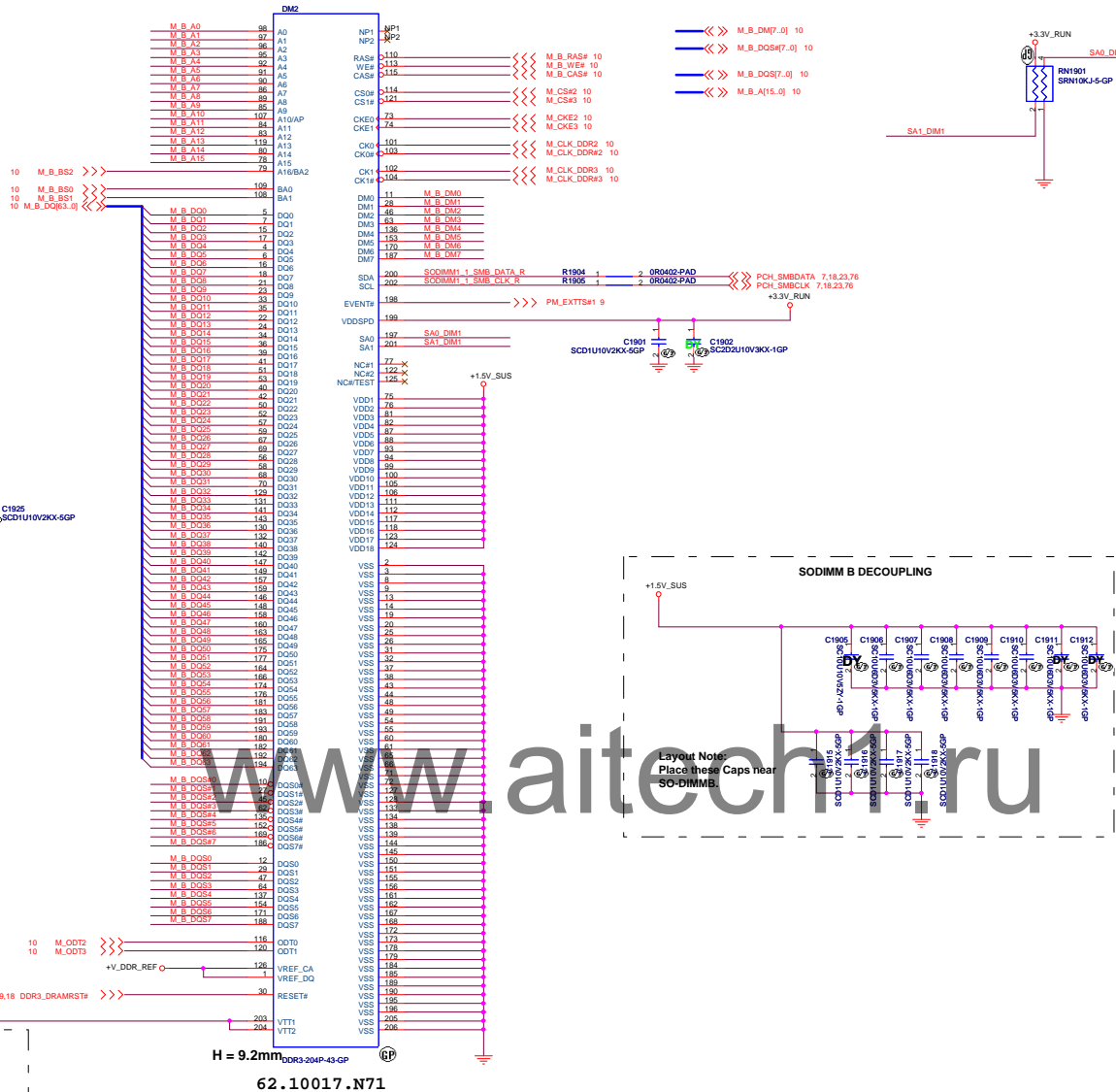


**Place these caps
close to VTT1 and
VTT2.**



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



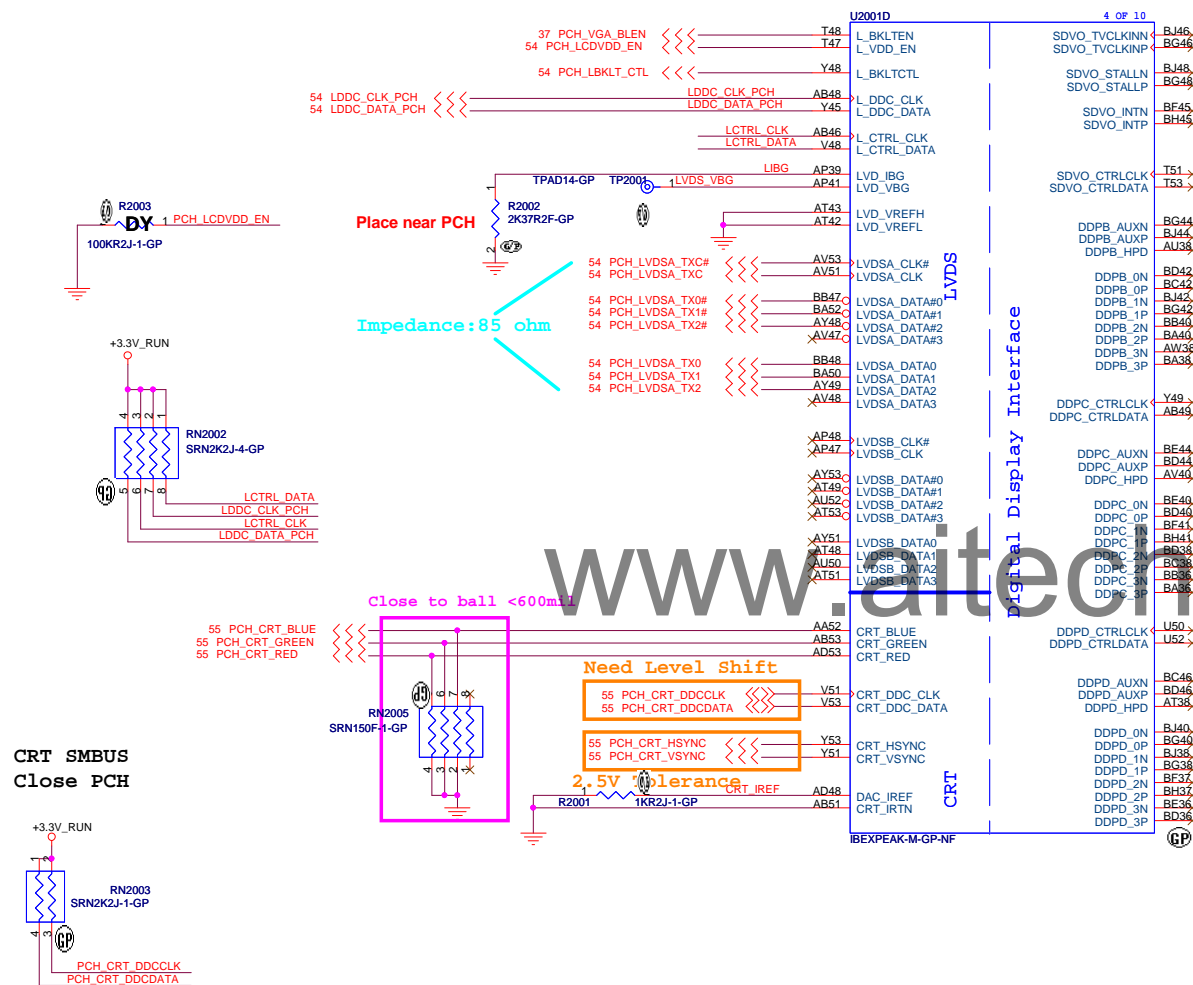
Layout Note:
Place these Caps near
SO-DIMMB.

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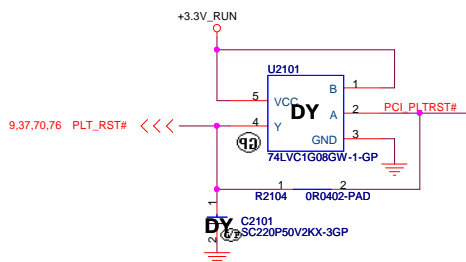
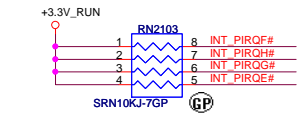
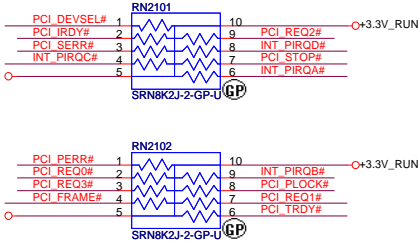


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DDR3-SODIMM2			
Size	Document Number		Rev
	DJ1 Calpella UMA		X
Date:	Thursday, April 22, 2010	Sheet	10 of 20

SSID = PCH



SSID = PCH

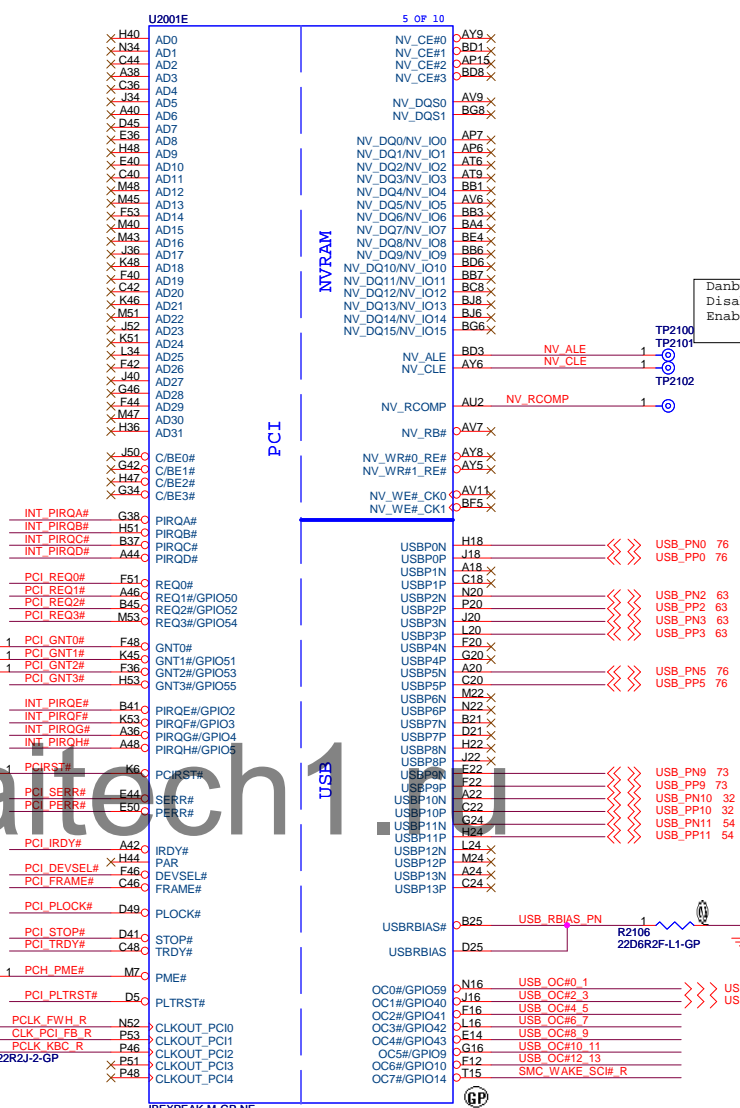
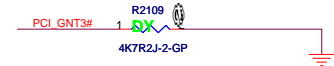


BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)



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A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 (I/O Board)
1	X
2	USB2
3	USB3
4	X
5	WLAN (I/O Board)
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

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Title: **PCH (PCI/USB/NVRAM)**

Size: Document Number: **DJ1 Calpella UMA** Rev: **X01**

Date: Thursday, April 22, 2010 Sheet 21 of 90

SSID = PCH

Option to "Disable" clkrun.
Pulling it down will keep the clks running.

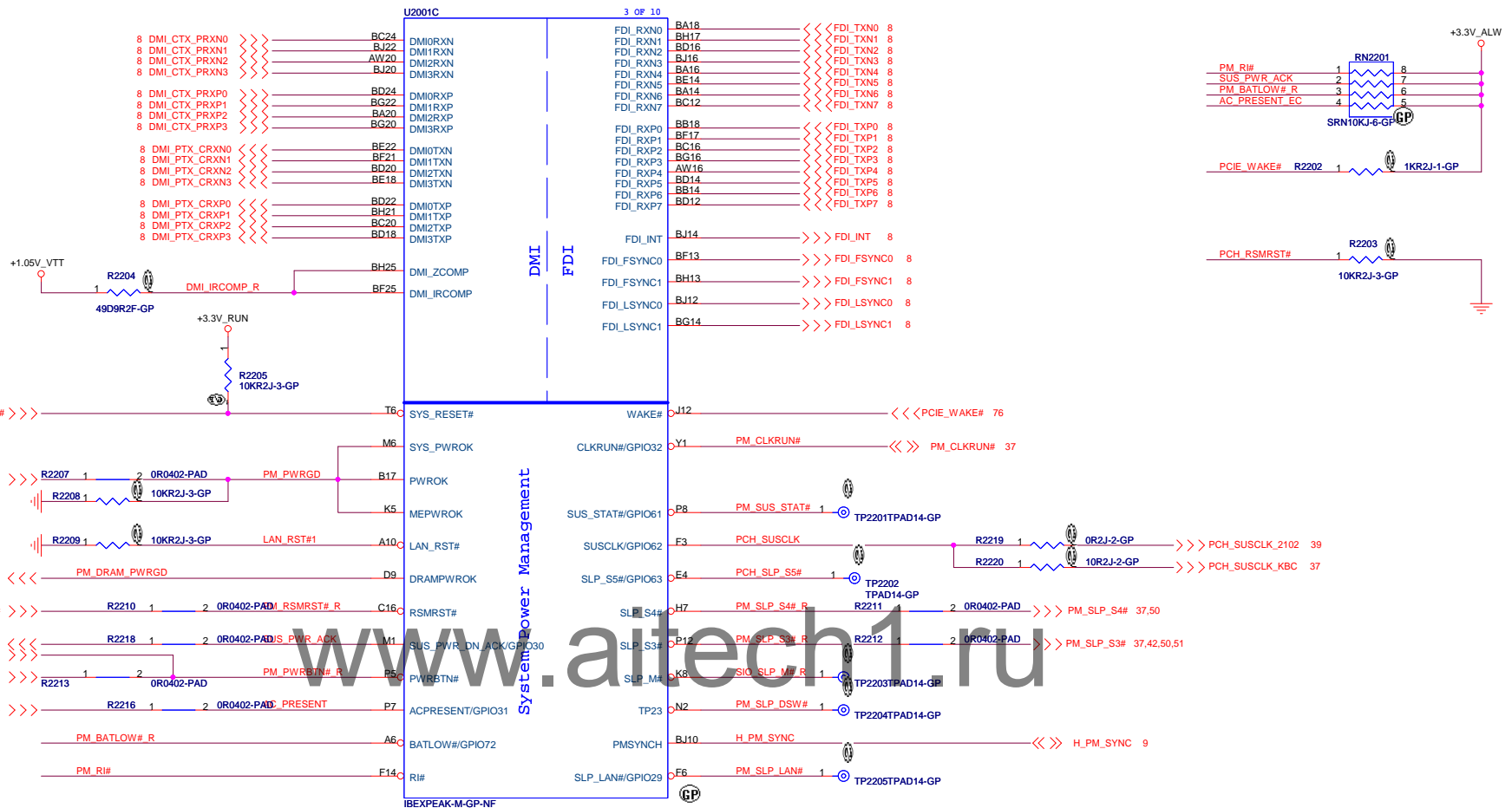
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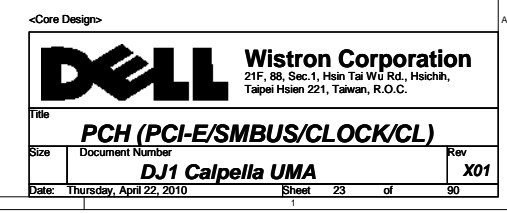
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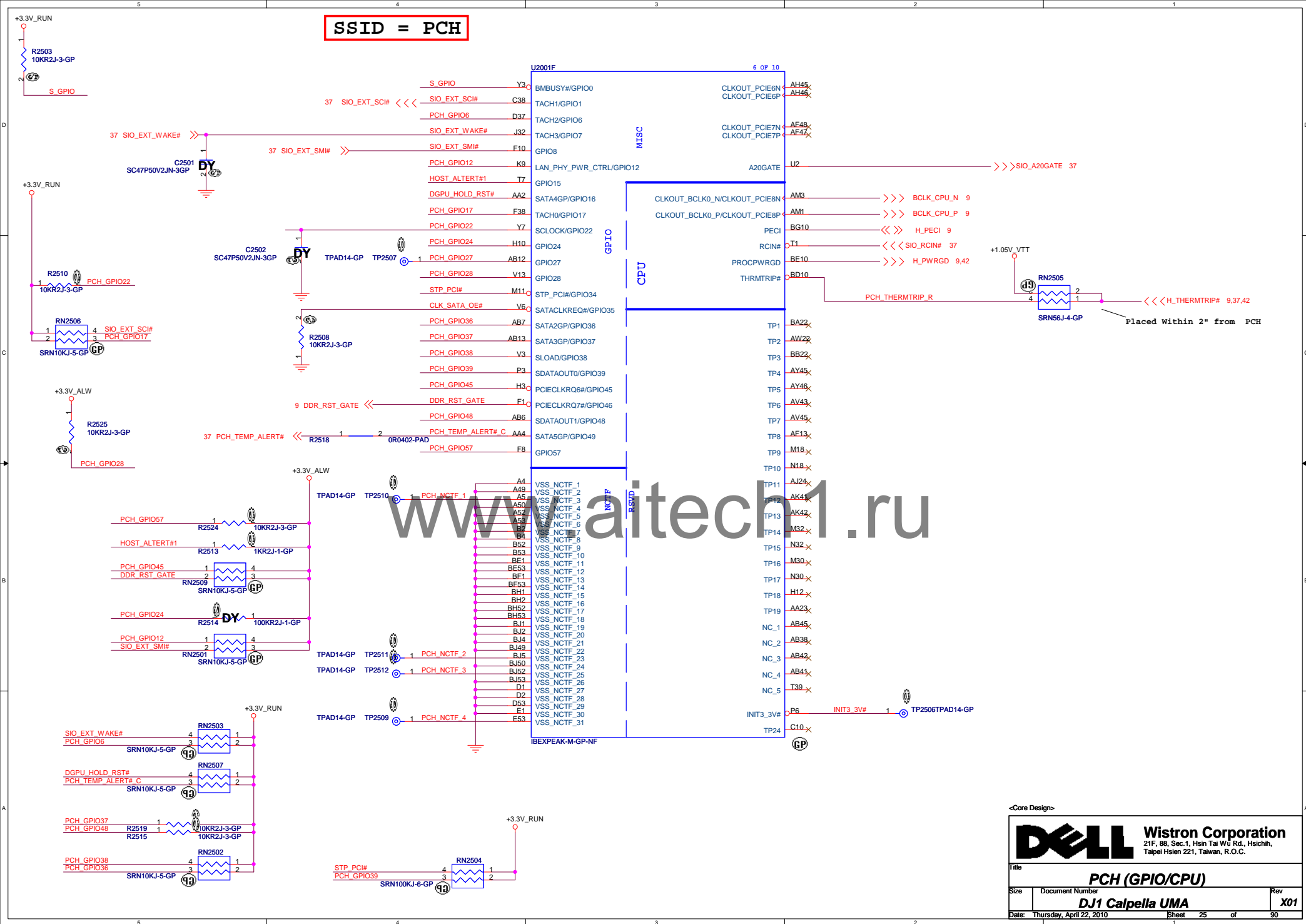
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Size	Document Number	Rev
	DJ1 Calpella UMA	X01
Date: Thursday, April 22, 2010		

Sheet 22 of 90

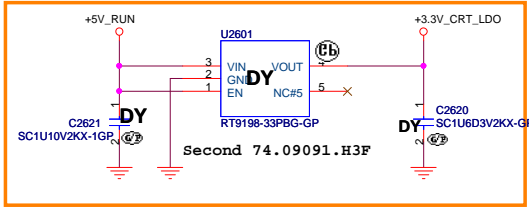


SSID = PCH





SSID = PCH

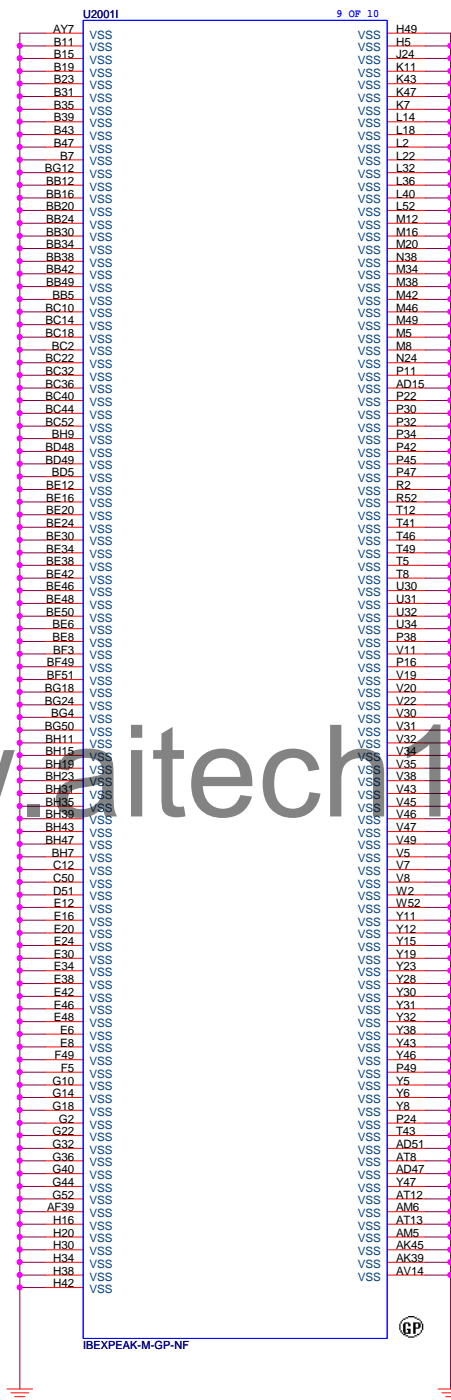
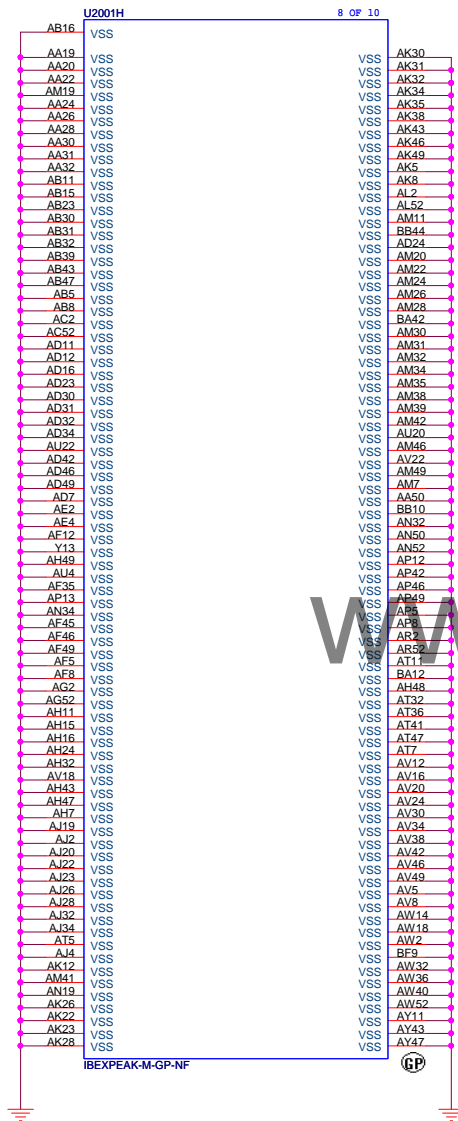


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Title	<i>PCH (POWER1)</i>
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Date: Wednesday, April 21, 2010 Sheet 26 of 90

SSID = PCH



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Title: **PCH (VSS)**


Size	Document Number	Rev
	DJ1 Calpella UMA	X01

Date: Friday, April 16, 2010 Sheet 28 of 90

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Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

Date: Friday, April 16, 2010	Sheet 29 of 90
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Size
A3

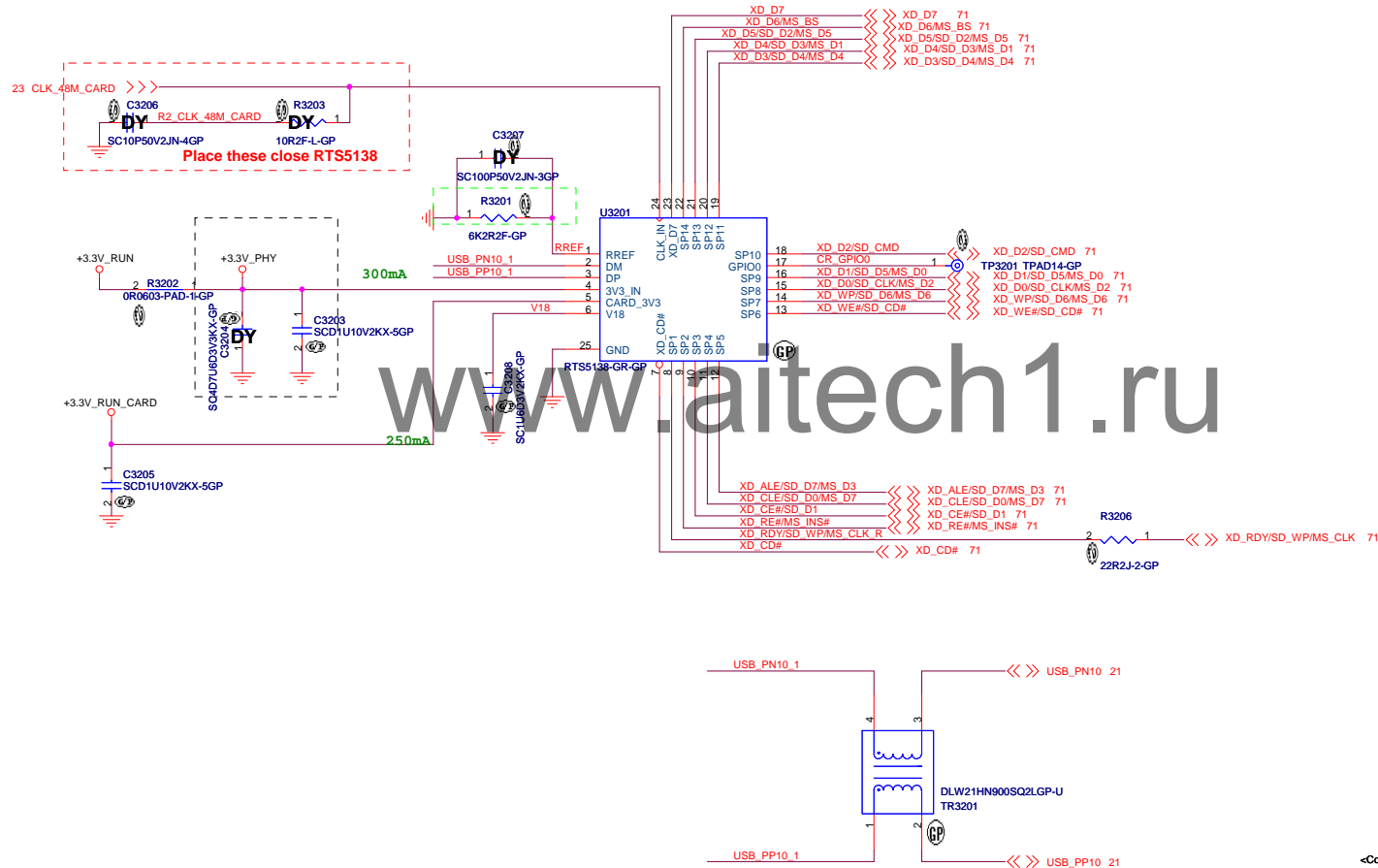
Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010

Rev
X01

Sheet 31 of 90


SSID = SDIO



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Reserved

Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01
Date: Friday, April 16, 2010		Sheet 33 of 90

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Reserved

Size

A3

Document Number

DJ1 Calpella UMA

Rev

X01


Date: Friday, April 16, 2010

Sheet 34 of 90

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Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010


Rev
X01

Sheet 35 of 90

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Title

Reserved

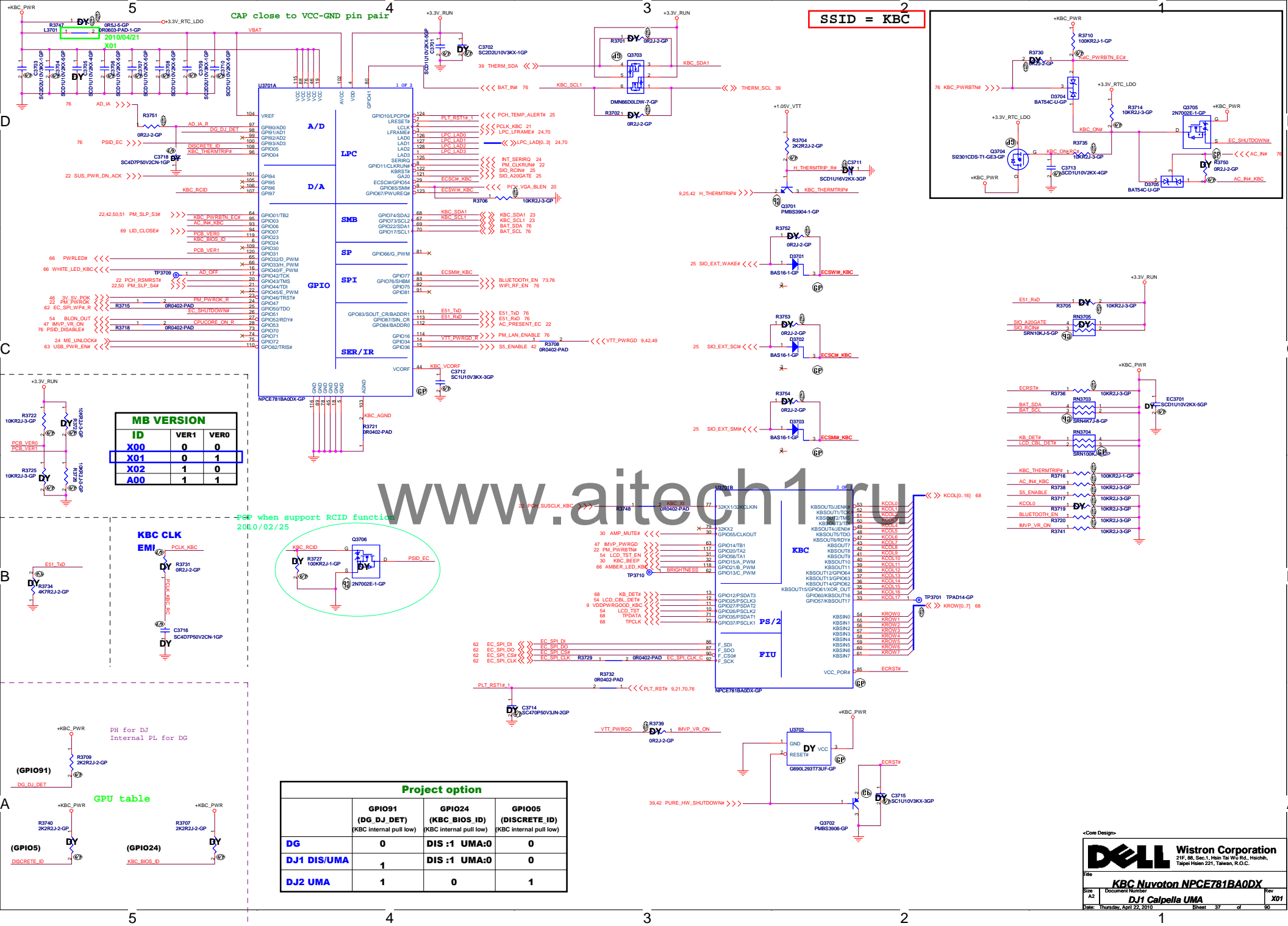
Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010

Rev
X01

Sheet 36 of 90




	Project option		
	GPIO91 (DG DJ DET) (KBC internal pull low)	GPIO24 (KBC BIOS ID) (KBC internal pull low)	GPIO05 (DISCRETE ID) (KBC internal pull low)
DG	0	DIS :1 UMA:0	0
DJ1 DIS/UMA	1	DIS :1 UMA:0	0
DJ2 UMA	1	0	1

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Reserved

Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010

Rev
X01

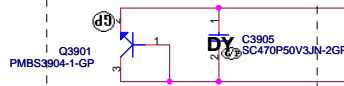
Sheet 38 of 90

SSID = Thermal

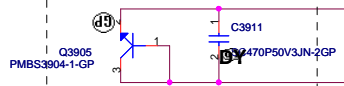
1. Place near CPU and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil trace width and 10 mil spacing.

C3905 must be near Q3901



C3904 must be near Q3905



2. System Sensor

Layout notice :
Both DN2 and DP2 routing 10 mil trace width and 10 mil spacing.

C3907 must be near Q3902



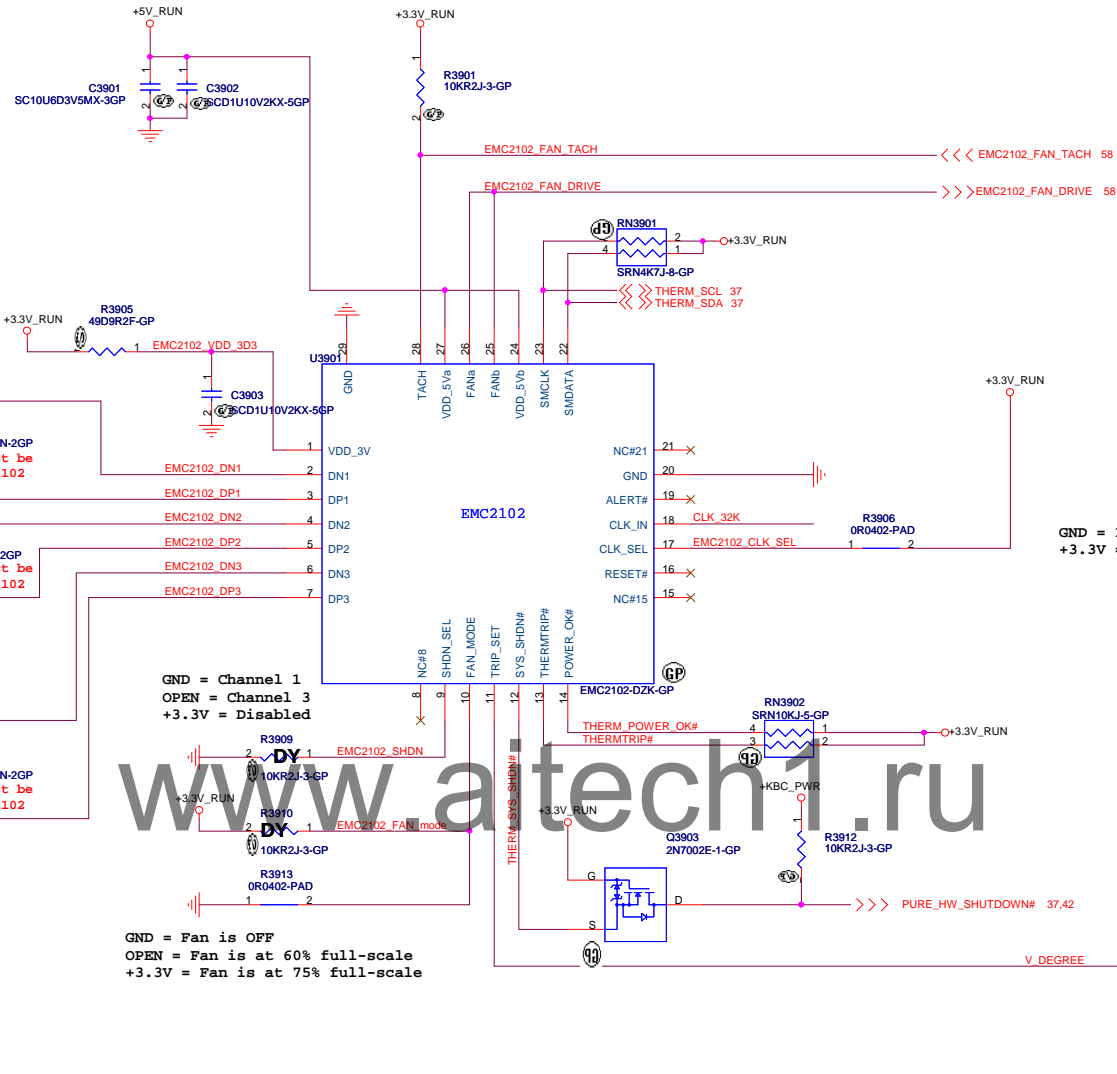
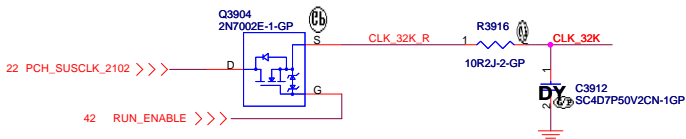
3. HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil trace width and 10 mil spacing.

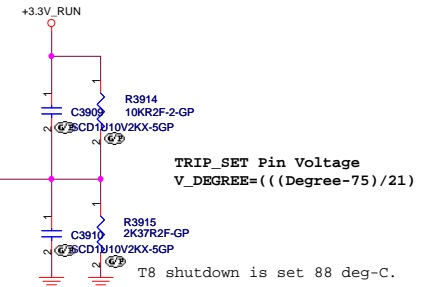


GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

32K suspend clock output



GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected



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Title: **Thermal/Fan Controller EMC2102**


Size: Custom Document Number: **DJ1 Calpella UMA** Rev: **X01**

Date: Thursday, April 22, 2010 Sheet 39 of 90

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Title

Reserved


Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

Date:	Friday, April 16, 2010	Sheet	40	of	90
		1			

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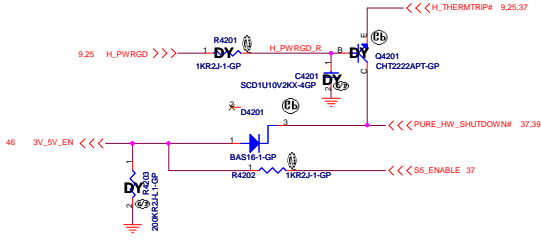
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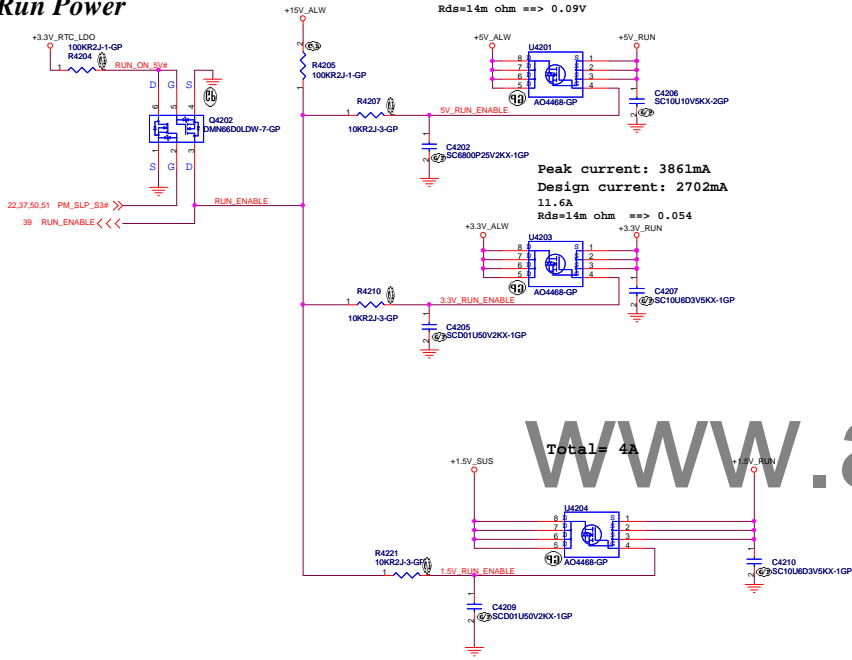
Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

Date:	Friday, April 16, 2010	Sheet	41	of	90
		1			

```
SSID = Reset.Suspend
```



Run Power



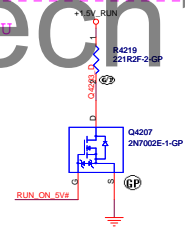
```
Peak current: 6370mA ( HD:1100 ODD:2500 )
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V
```

$$\text{Total} = 4A$$

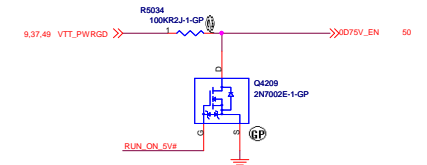
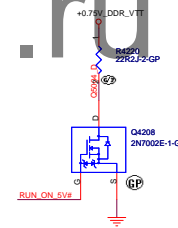
The diagram shows a protein structure with several highlighted regions and labels:

- Total= 4A**: A label on the left side of the structure.
- +13V_RUN**: A label pointing to a red circle on the left side of the structure.
- +13V_RUN**: A label pointing to a red circle on the right side of the structure.
- For GPU**: A label in the center of the structure, enclosed in a dashed pink box.
- 425302, 425302**: A label on the far right side of the structure.
- +0.75V_DDR_VTT**: A label pointing to a red circle on the far right side of the structure.
- R4219**: A label pointing to a red circle on the right side of the structure.
- 221R2F-2GP**: A label pointing to a red circle on the right side of the structure.
- R4220**: A label pointing to a red circle on the right side of the structure.
- 22R2F-2**: A label pointing to a red circle on the right side of the structure.

For CPU



425302_425302_Calpella_S3PowerReduction_WhitePape
Revision 0.7



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Title			
Power Plane Enable			
Size A2	Document Number DJ1 Calpella UMA		Rev X01
Date: Thursday, April 22, 2010		Sheet 42 of	90

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Title

Reserved

Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010


Rev
X01

Sheet 43 of 90

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Title

Reserved


Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

Date:	Friday, April 16, 2010	Sheet	44	of	90
		1			

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Reserved

Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010

Rev
X01

Sheet 45 of 90

Design Current = 9.07A
14.25A < OCP < 16.84A

Design Current = 8.4A
13.32A < OCP < 15.75A

TONESEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

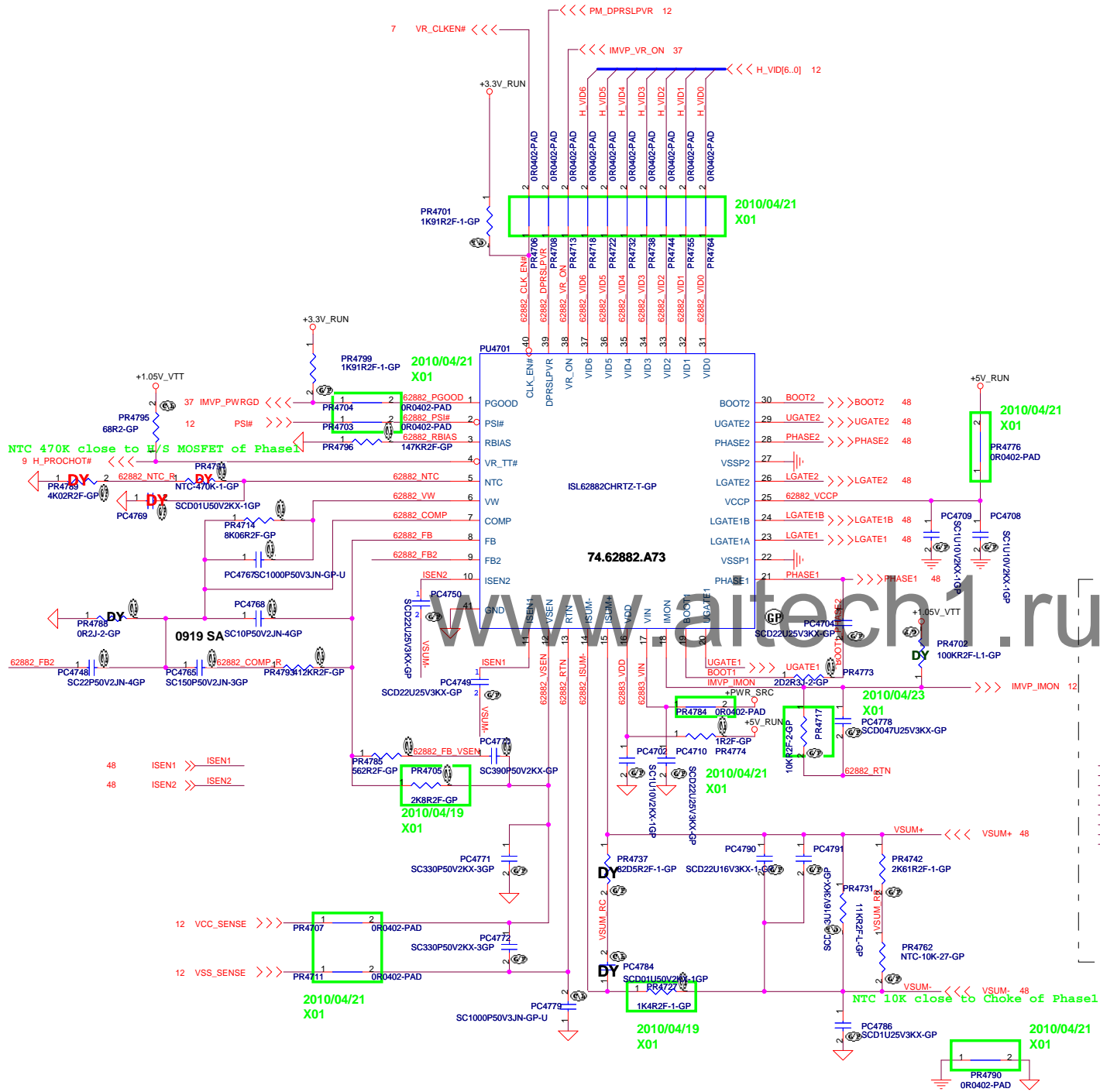
TONESEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only
EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

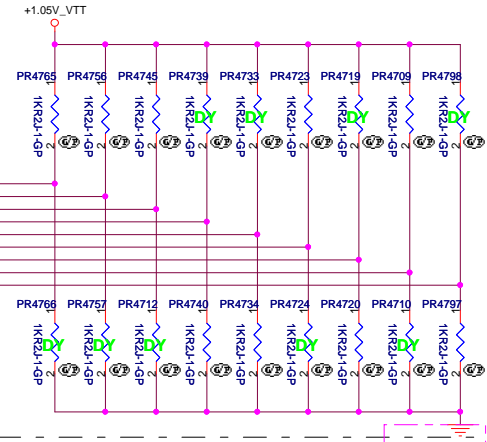
<Core Design>



File	TPS51125_5V/3D3V		
Doc Number	DJ1 Calpella UMA		
Rev	X01		
Date	Thursday, April 22, 2010	Sheet	48 of 90



Intel support POC (power on current).

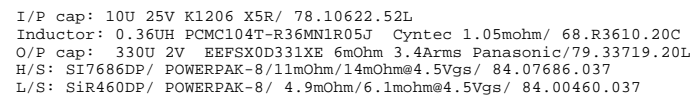
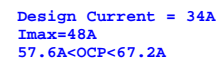


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ISL62883 CPU CORE

Size A3 Document Number **Berry** Rev **X01**

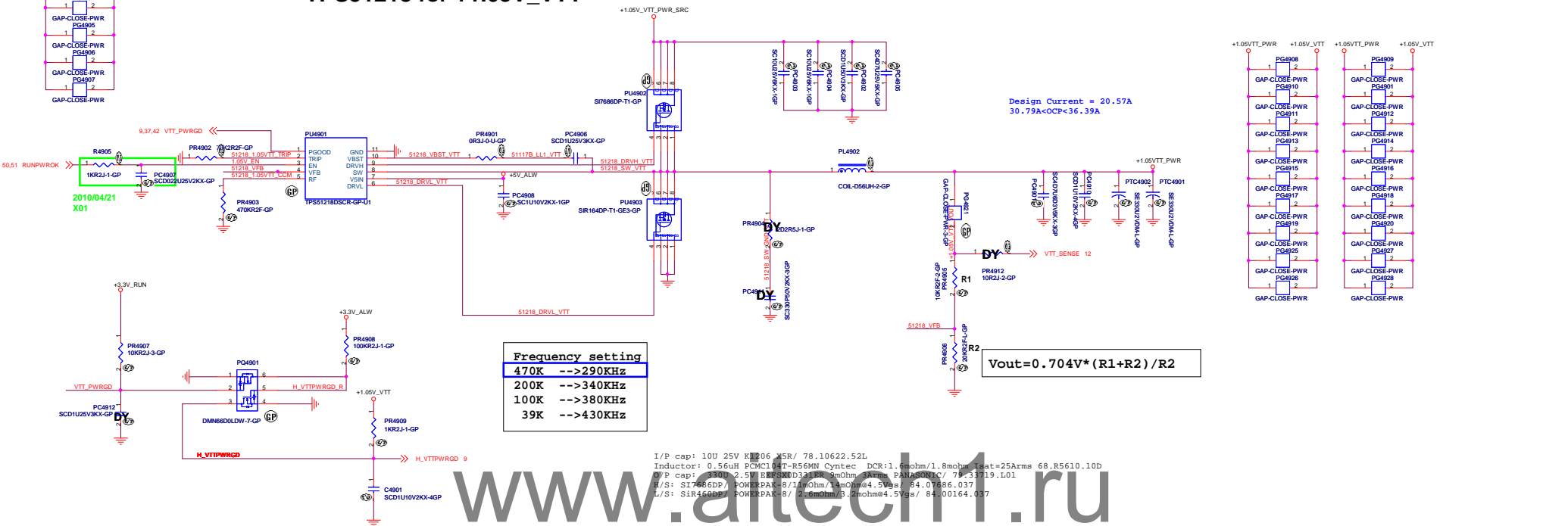
Date: Monday, April 26, 2010 Sheet 47 of 90



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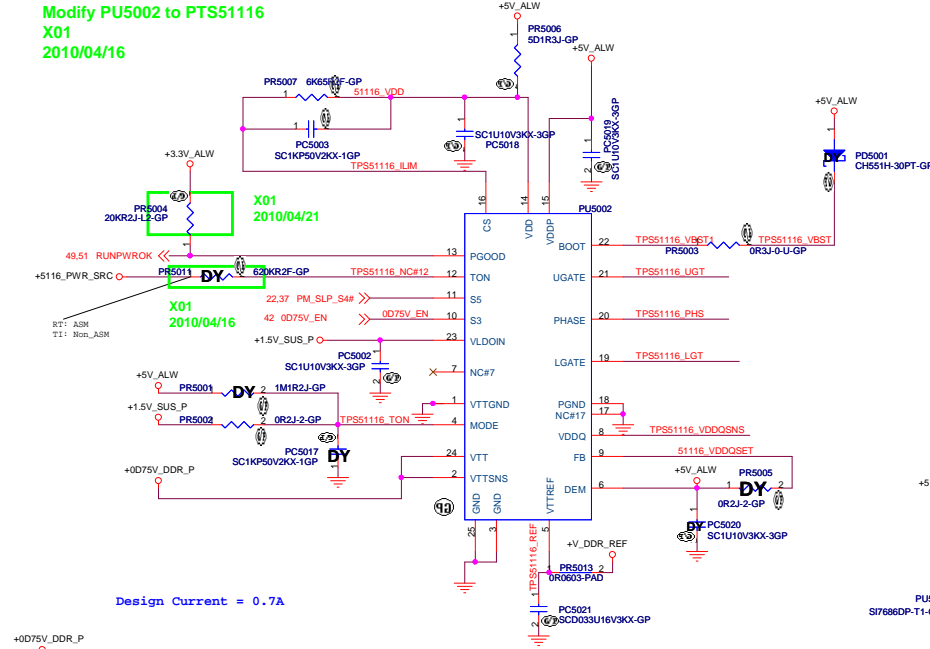
Sheet 48 of 90

TPS51218 for +1.05V_VTT

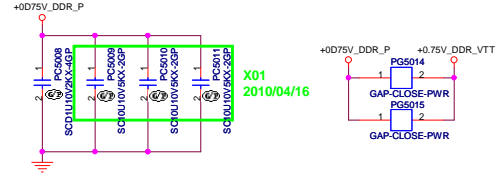


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Modify PU5002 to PTS51116
X01
2010/04/16



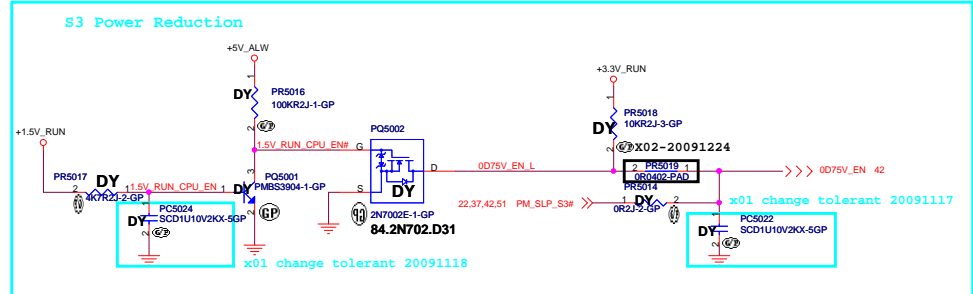
Design Current = 0.7A



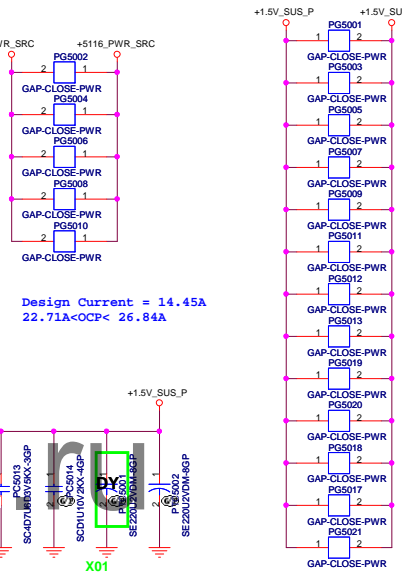
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5uH PCMC104T-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J
O/P cap: 220U 2V EEPX0D221ER 15mohm 2.7Arms PANASONIC/ 79.27219.20L
H/S: Si7686DP/ POWERPAK-8/ 11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz



Design Current = 14.45A
22.71A<OCP< 26.84A



Close to VFB Pin (pin5)

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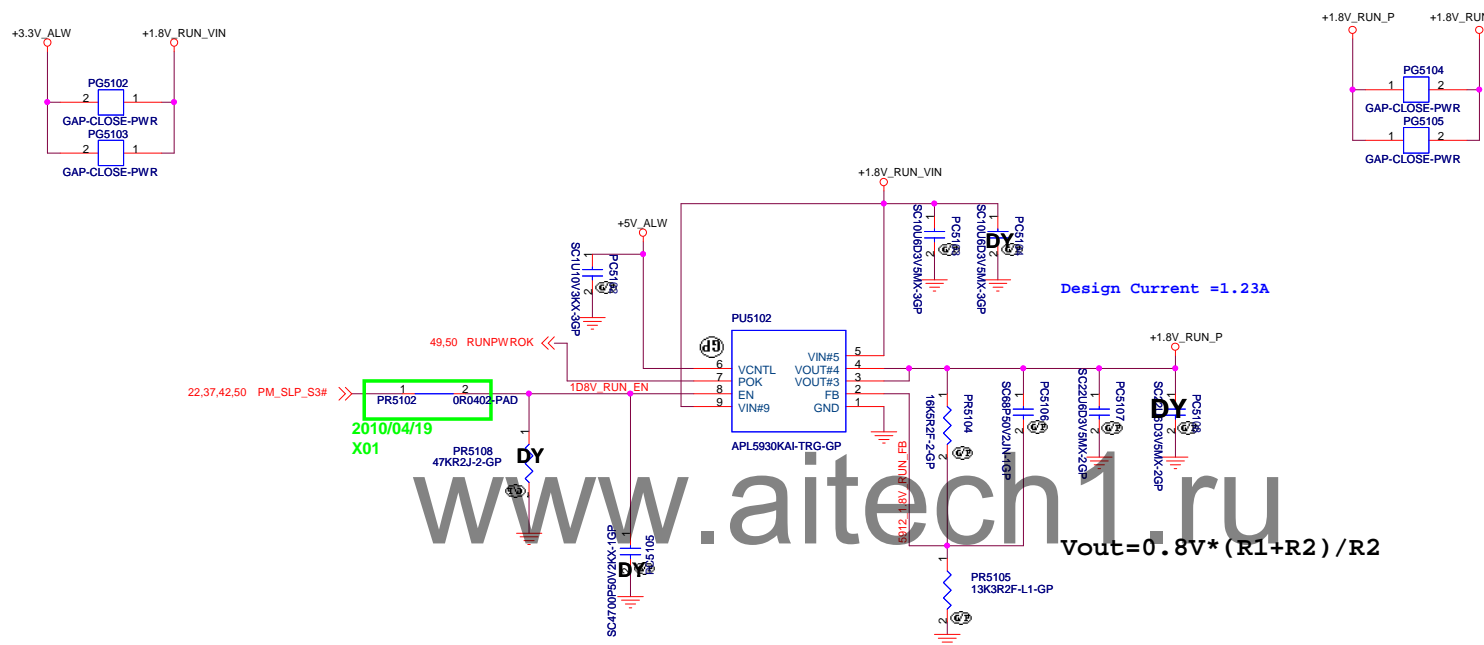
File: **TPS51116 +1.5V SUS**

Size: Document Number: **DJ1 Calpella UMA** Rev: **X01**

Date: Thursday, April 22, 2010 Sheet: 50 of 90

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



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Title

APL5930 +1.8V RUN

Size
A3

Document Number

DJ1 Calpella UMA

Rev

X01


Date: Thursday, April 22, 2010

Sheet 51 of 90

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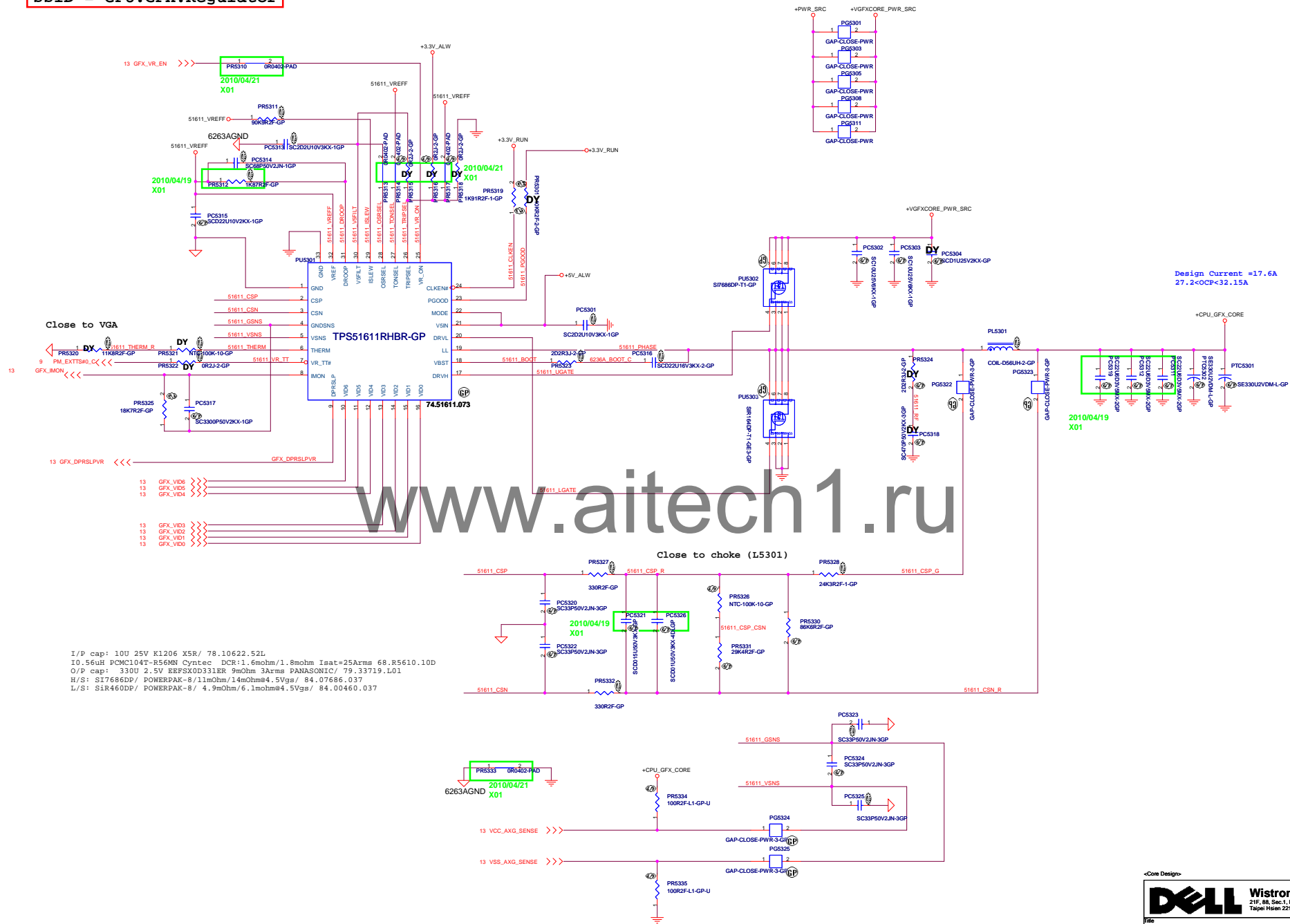
Title

Reserved

Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

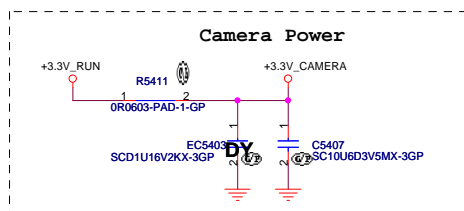
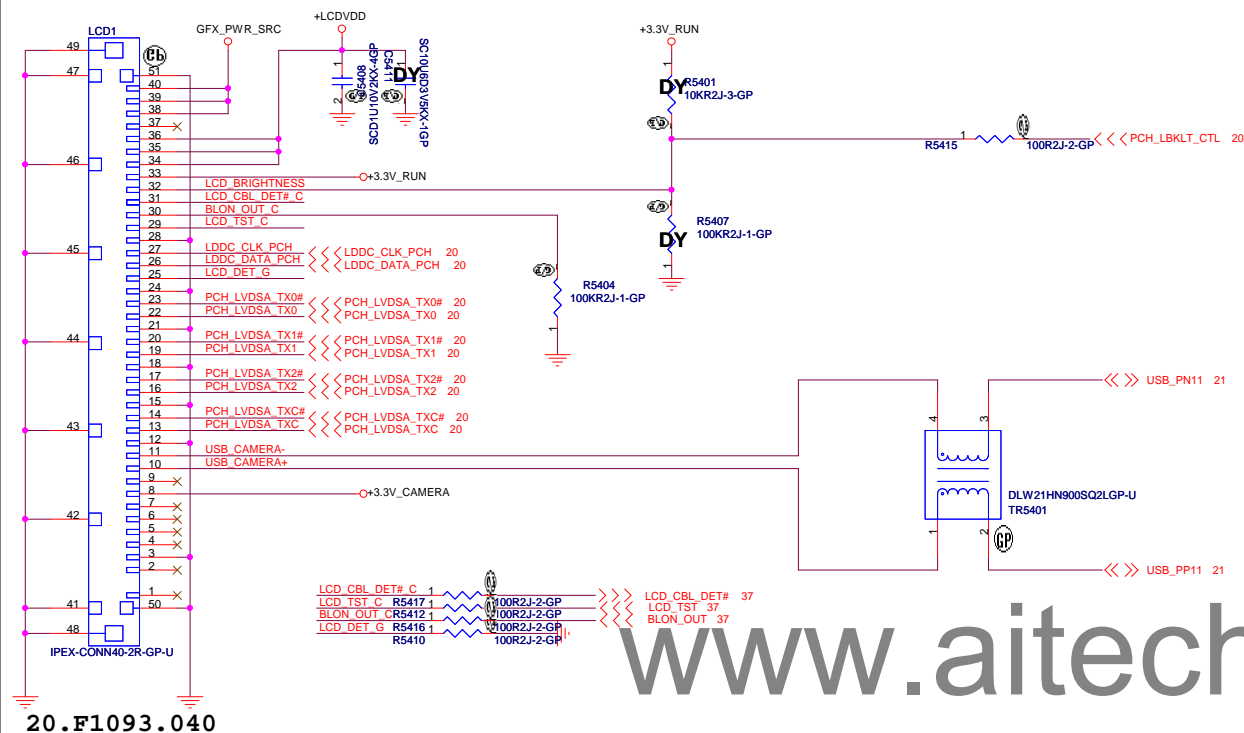
Date:	Friday, April 16, 2010	Sheet	52	of	90
		1			


```
SSID = CPU.GFX.Regulator
```



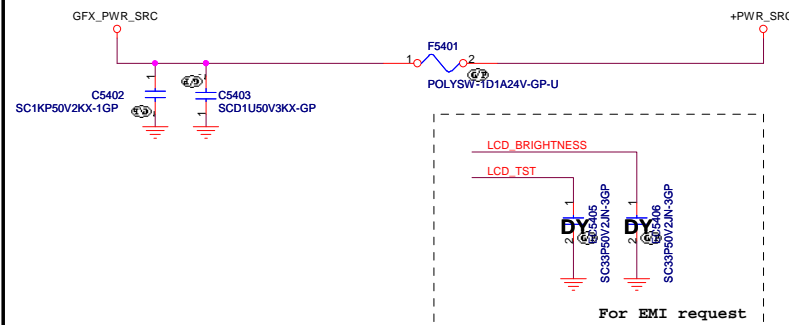
SSID = VIDEO

LVDS CONNECTOR



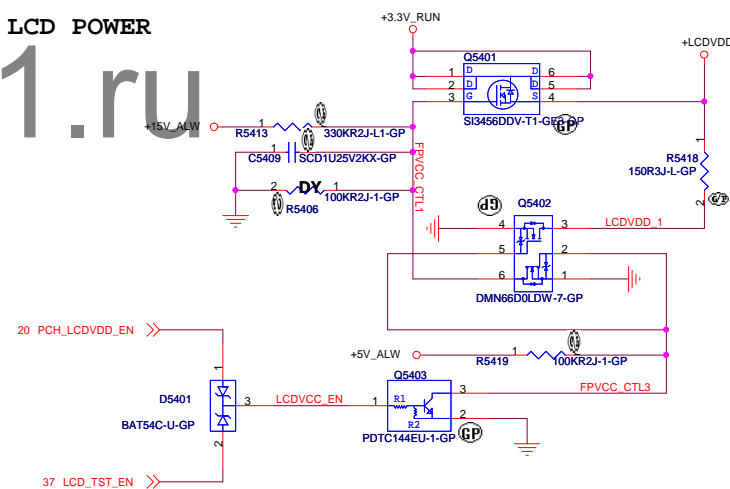
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

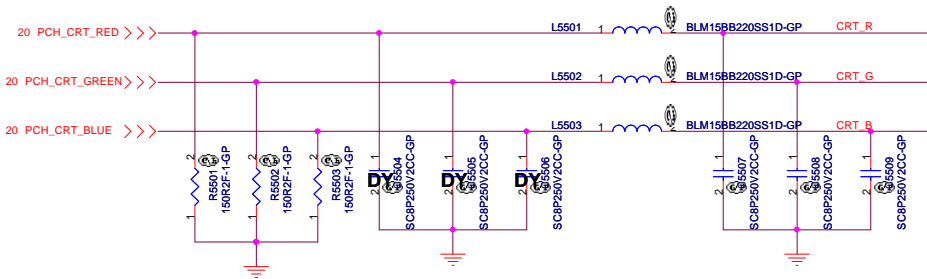
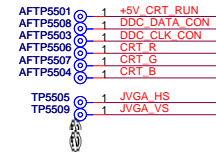
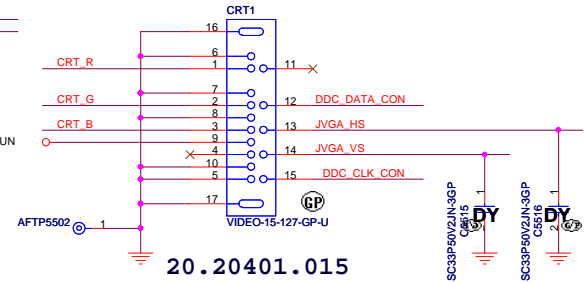
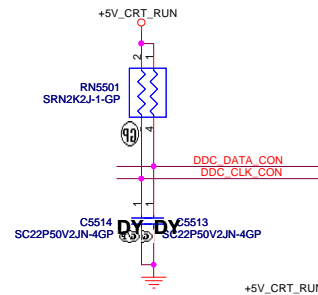
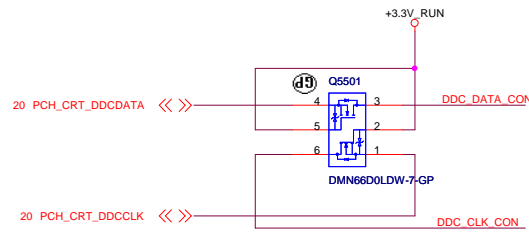
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Title		
LCD/Inverter Connector		
Size A3	Document Number DJ1 Calpella UMA	Rev X01
Date: Monday, April 26, 2010	Sheet 54	of 90

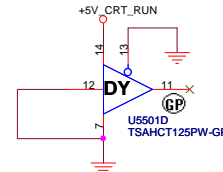
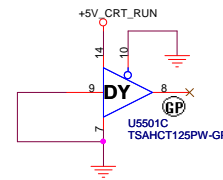
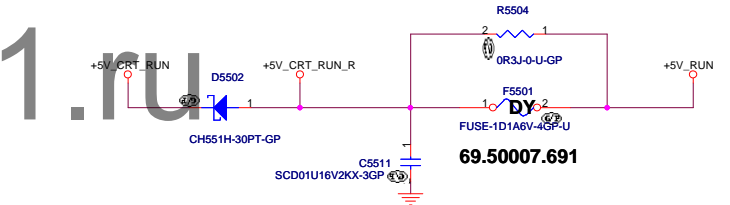
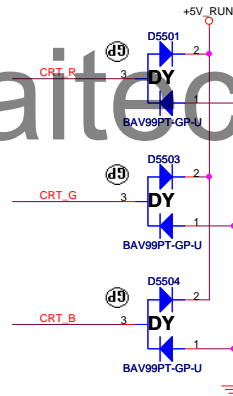
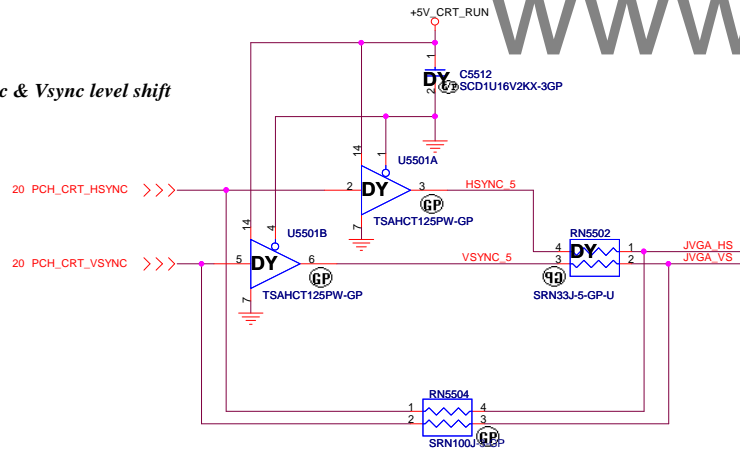
SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



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Title: **CRT Connector**

Size: Document Number: **DJ1 Calpella UMA** Rev: **X01**


Date: Thursday, April 22, 2010 Sheet 55 of 90

CLOSE TO
TRANSFORMER

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Title

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Size	Document Number	Rev
A3	DJ1 Calpella UMA	X01

Date:	Friday, April 16, 2010	Sheet	56	of	90
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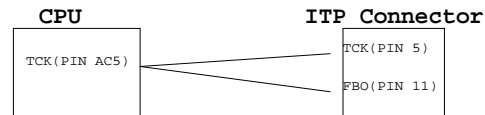
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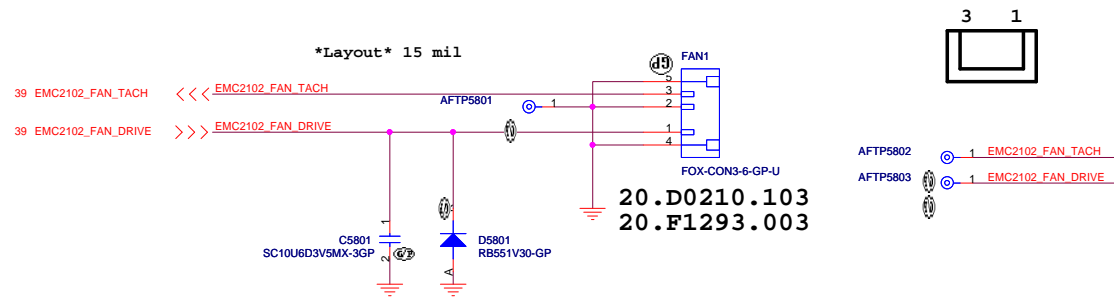
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDMI			
Size	Document Number		Rev
A3	DJ1 Calpella UMA		X01
Date:	Friday, April 16, 2010		Sheet 57 of 90

SSID = Thermal

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



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Fan Connector



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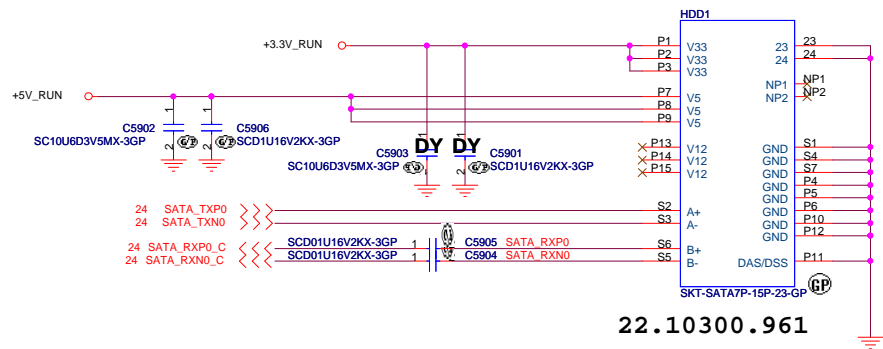
ITP/Fan Connector

DJ1 Calpella UMA

Sheet

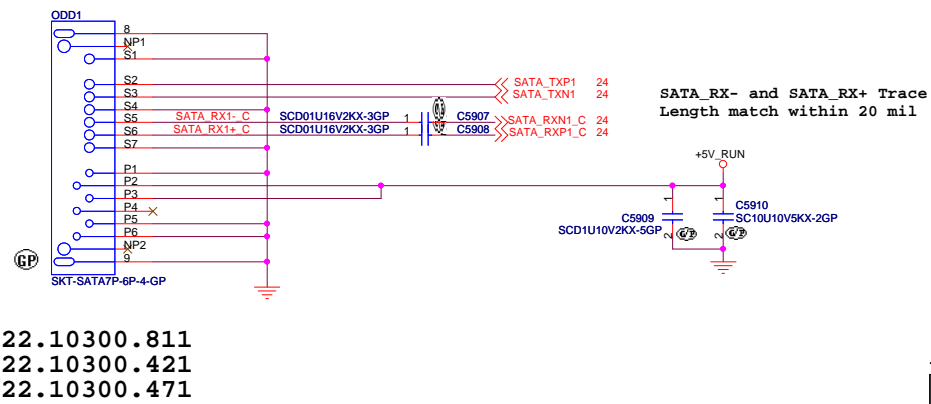
Rev
X01

SATA HDD Connector



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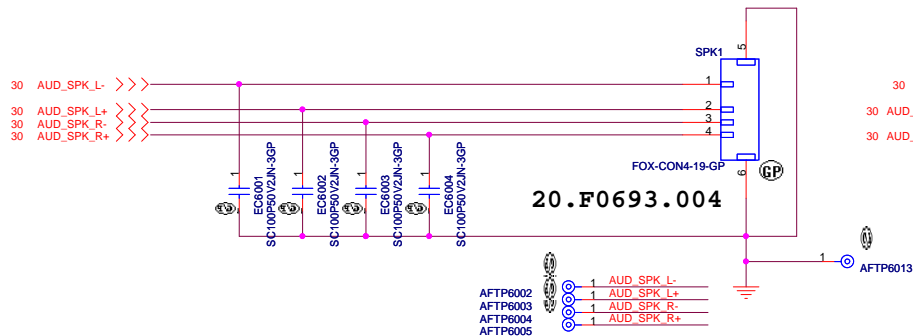
ODD Connector



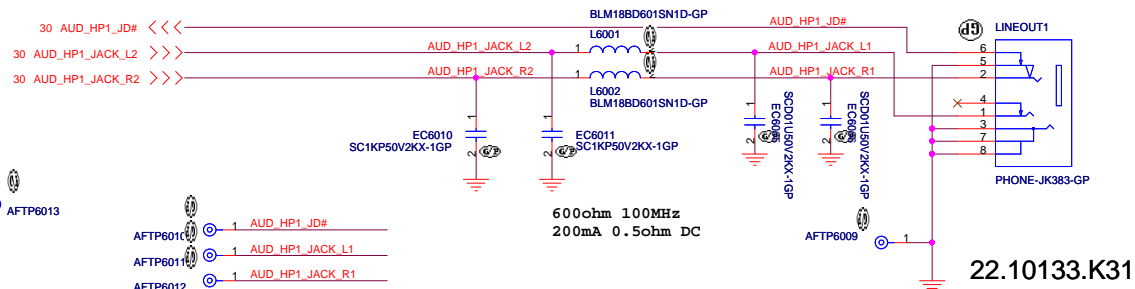
SSID = AUDIO

Speaker Connector

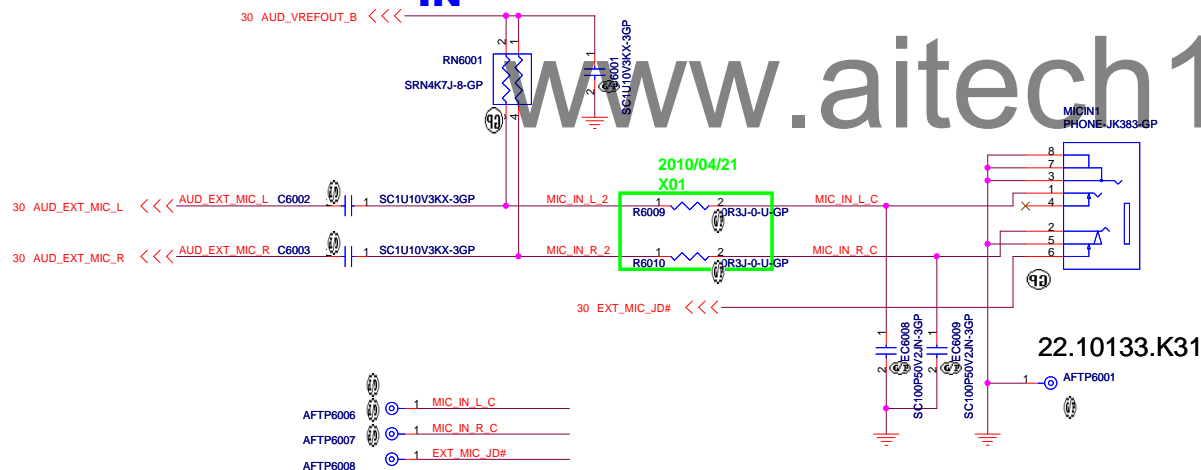
20.F0711.004



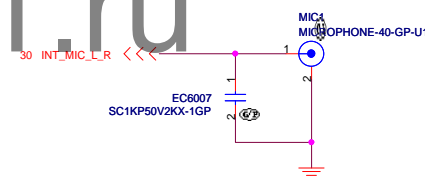
LINE1 OUT



MIC IN



Internal Microphone



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Title

Audio Jack

Size
A3

Document Number

DJ1 Calpella UMA

Rev

X01


Date: Thursday, April 22, 2010

Sheet 60 of 90

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Title

Reserved

Size

A3

Document Number

DJ1 Calpella UMA

Rev

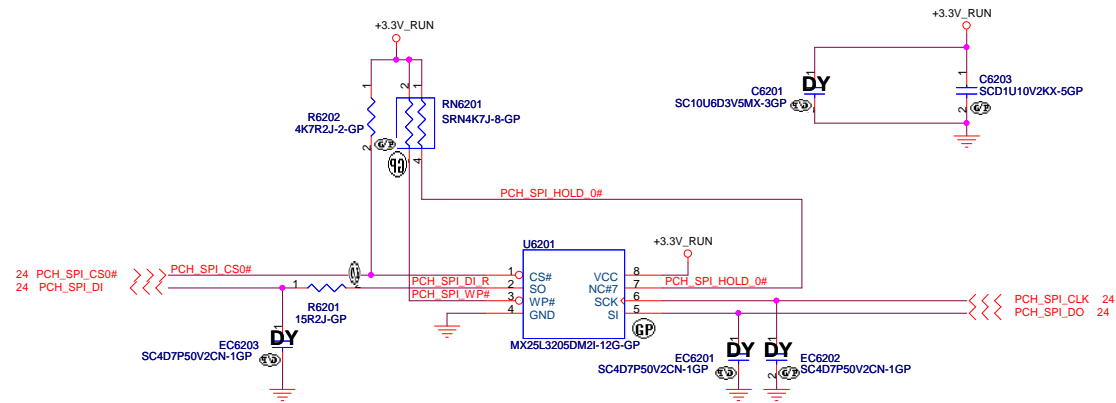
X01

Date: Friday, April 16, 2010

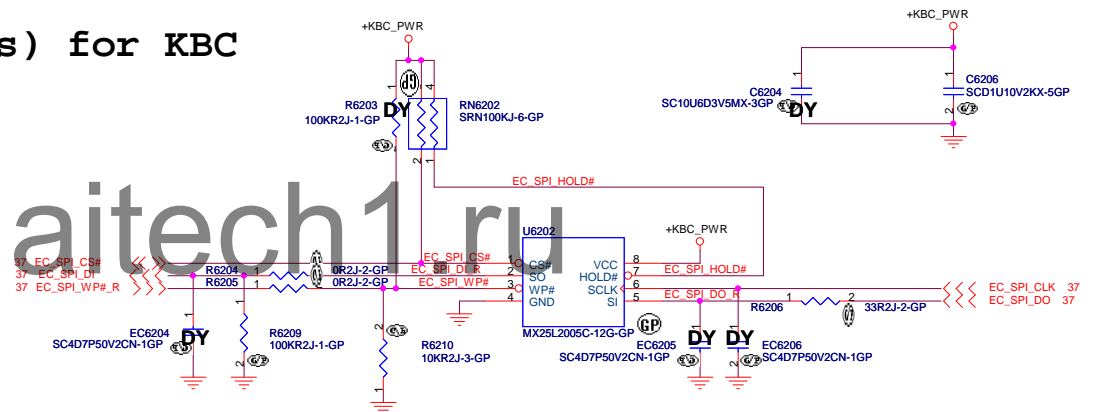
Sheet 61 of 90

SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

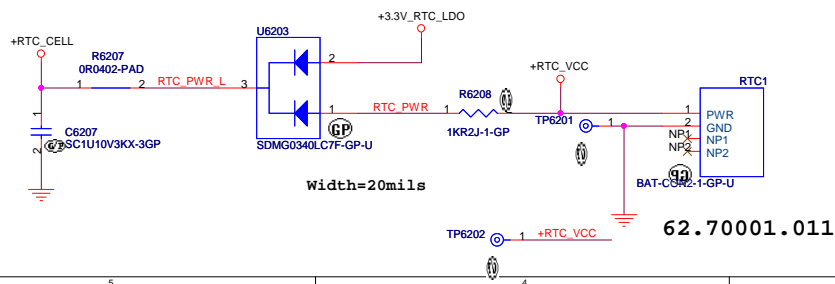


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



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Title		Flash/RTC	
Size	Document Number	Rev	
A3	DJ1 Calpella UMA	X01	
Date:	Thursday, April 22, 2010	Sheet	62 of 90

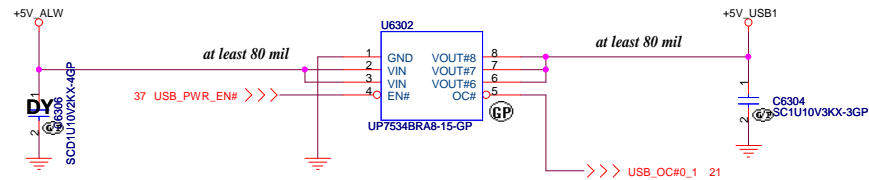
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IO Board USB Power

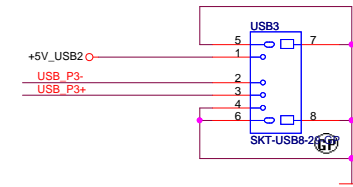
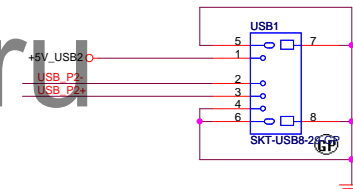
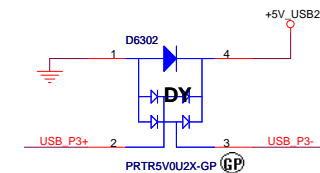
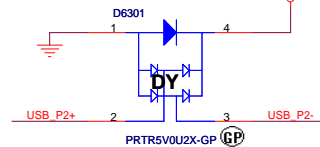
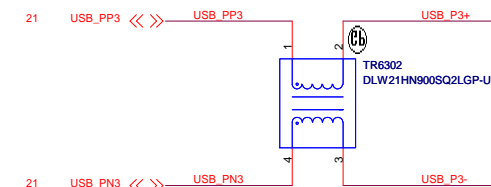
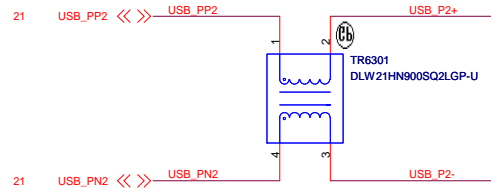
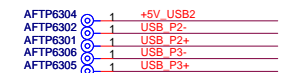
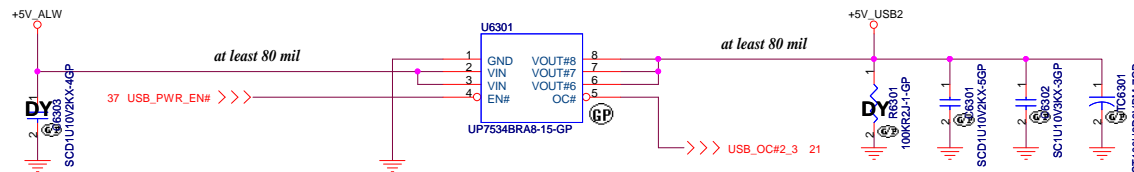
USB POWER SW

Main UP7534BRA8-15 P/N:74.07534.079

SEC AP2101MPG-13 P/N: 74.02101.079



Right USB Power



22.10254.451


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Title		USB	
Size	Document Number	Rev	
	DJ1 Calpella UMA	X01	
Date: Thursday, April 22, 2010	Sheet 63	of 90	

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A3	DJ1 Calpella UMA		X01
Date:	Friday, April 16, 2010		Sheet 64 of 90

(Blanking)

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Reserved

Size
A3

Document Number
DJ1 Calpella UMA

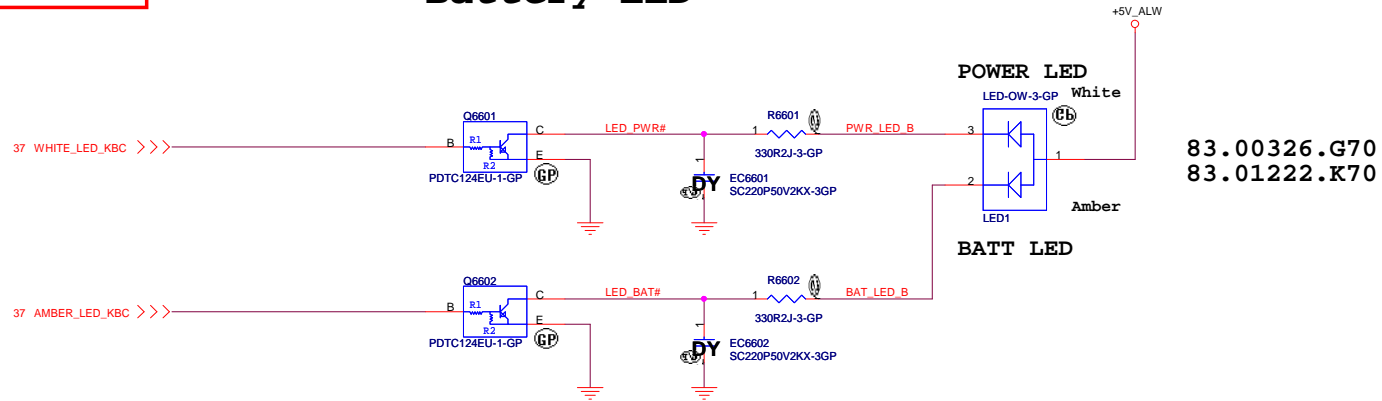
Date: Friday, April 16, 2010

Rev
X01

Sheet 65 of 90

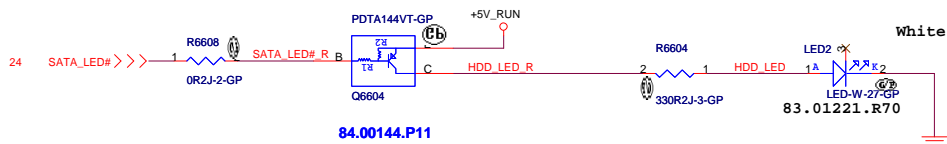
SSID = User.Interface

Battery LED

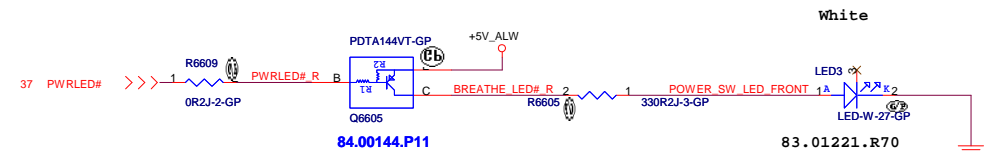


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HDD LED



BREATHE PWR LED (Front)



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LED

Size
A3

Document Number

DJ1 Calpella UMA

Rev

X01


Date: Thursday, April 22, 2010

Sheet 66 of 90

(Blanking)

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Reserved

Size
A3

Document Number
DJ1 Calpella UMA

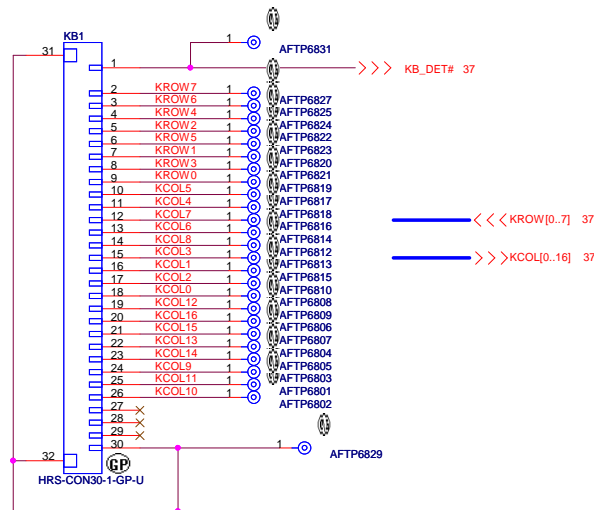
Date: Friday, April 16, 2010

Rev
X01

Sheet 67 of 90

SSID = KBC

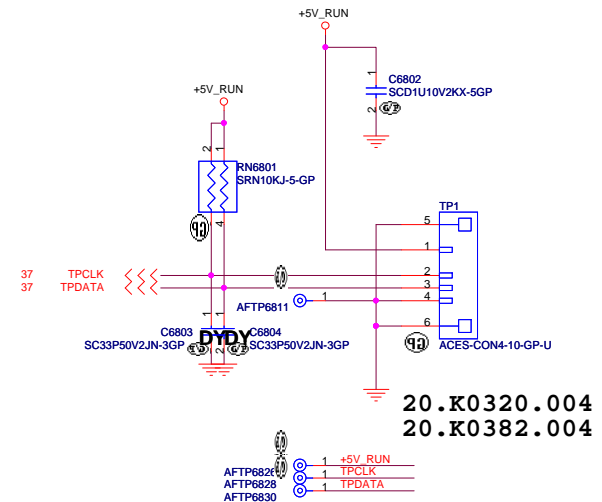
Internal KeyBoard Connector



Main 20.K0259.030
20.K0461.030
20.K0421.030

SSID = Touch.Pad

TouchPad Connector

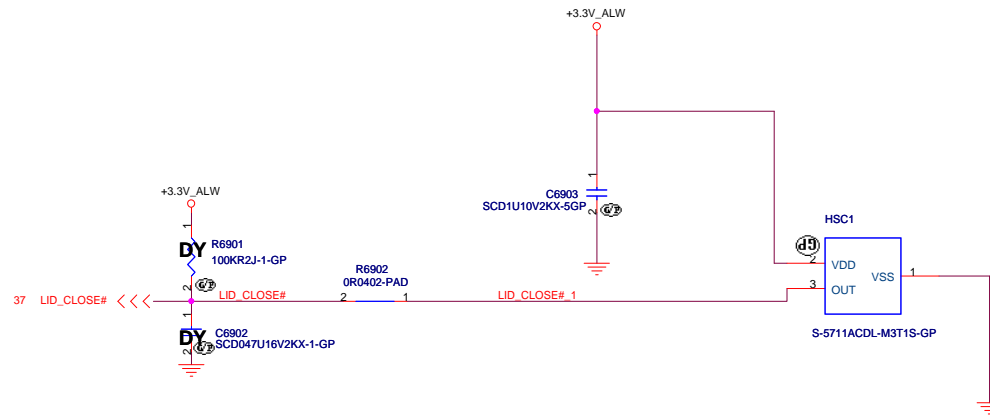


20.K0320.004
20.K0382.004

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Title			
Key Board/Touch Pad			
Size	Document Number	Rev	
A3	DJ1 Calpella UMA	X01	
Date:	Thursday, April 22, 2010	Sheet	68 of 90



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Title

Hall Sensor

Size
A3

Document Number

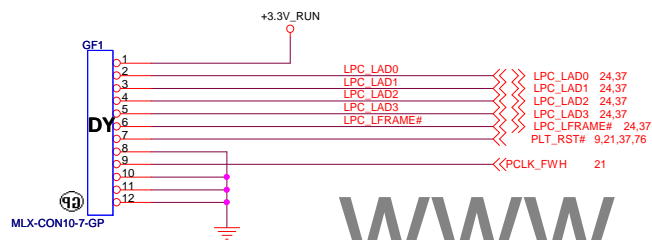
DJ1 Calpella UMA

Rev

X01

Date: Thursday, April 22, 2010

Sheet 69 of 90



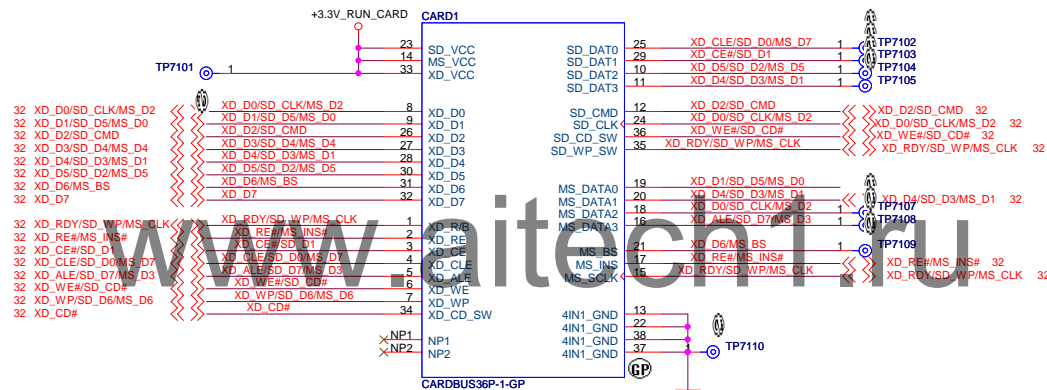
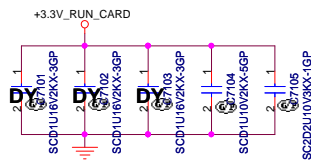
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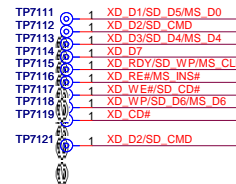
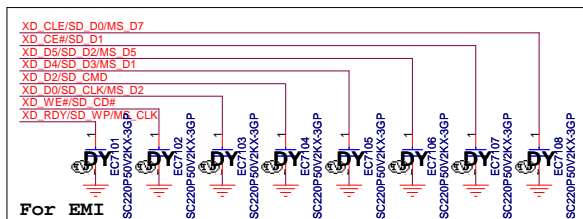
Title		
Reserved		
Size A3	Document Number DJ1 Calpella UMA	Rev X01
Date: Thursday, April 22, 2010	Sheet 70 of 90	1

SSID = SDIO

SD/XD/MS Card Reader



20.I0109.001
20.I0081.011



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Title: **CARD Reader CONN**
Size: A3 Document Number: **DJ1 Calpella UMA** Rev: **X01**
Date: Thursday, April 22, 2010 Sheet 71 of 90

(Blanking)

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Title

Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010

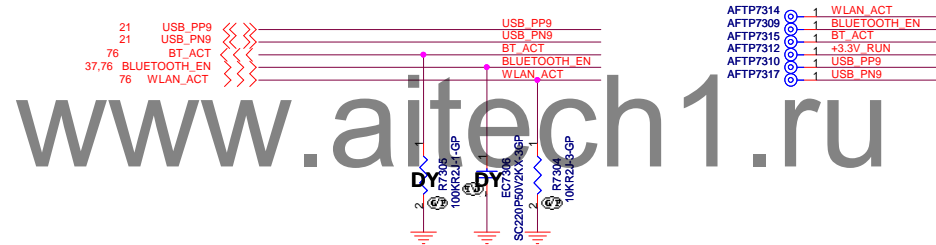
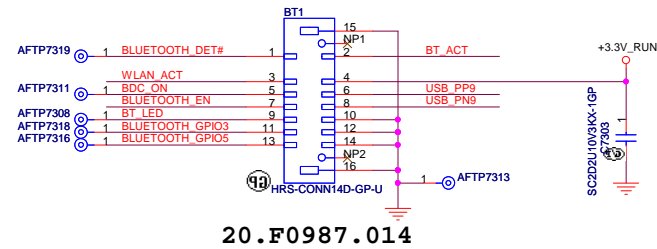
RESERVED

Rev
X01

Sheet 72 of 90

SSID = User.Interface

Bluetooth Module conn.



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Title

Bluetooth

Size
A3

Document Number

DJ1 Calpella UMA

Rev
X01


Date: Thursday, April 22, 2010

Sheet 73 of 90

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Title

Reserved

Size
A3

Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010


Rev
X01

Sheet 74 of 90

(Blanking)

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Title

Reserved

Size
A3

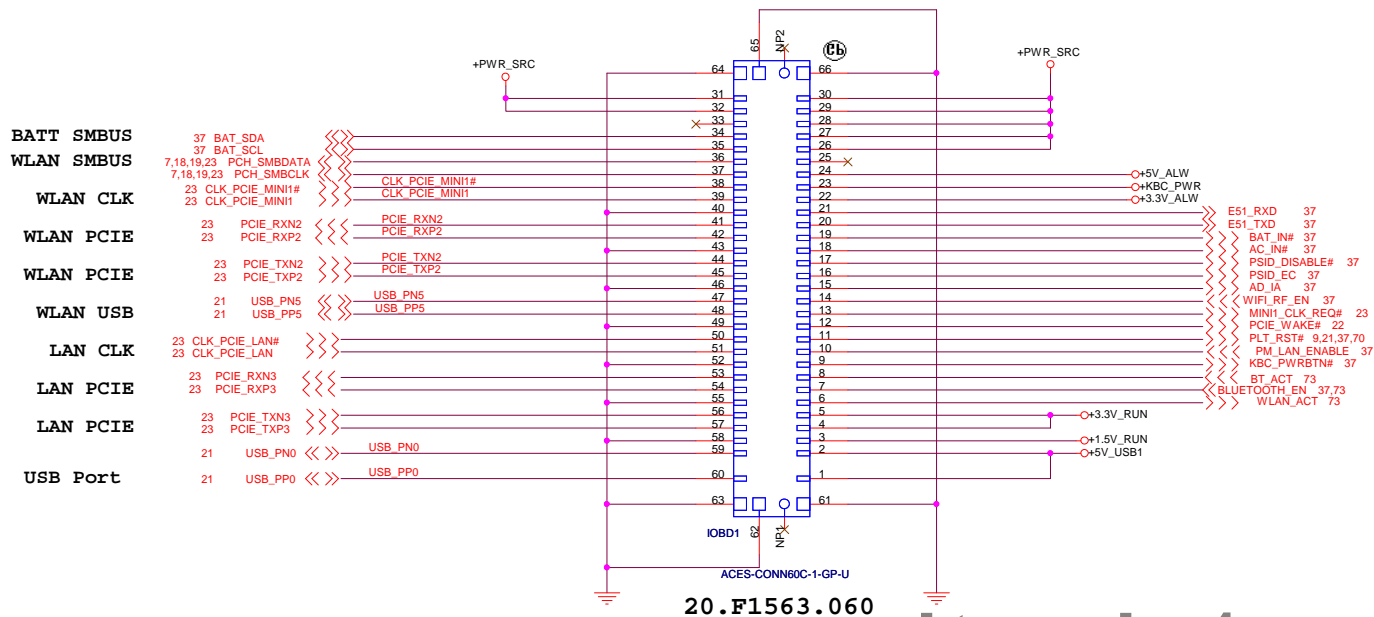
Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010

Rev
X01

Sheet 75 of 90


SSID = PWR.Support



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Title			
Reserved			
Size A3	Document Number DJ1 Calpella UMA		Rev X01
Date: Friday, April 16, 2010	Sheet	77	of 90

(Blanking)

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Reserved

Size
A3

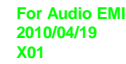
Document Number
DJ1 Calpella UMA

Date: Friday, April 16, 2010


Rev
X01

Sheet 78 of 90

2010/04/20
X01




2010/04/20
X01

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Title			
UNUSED PARTS/EMI Capacitors			
Size A3	Document Number DJ1 Calpella UMA	Rev X01	
Date:	Thursday, April 22, 2010	Sheet	79 of 90

SSID = VIDEO

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Title			
Reserved			
Size	Document Number		Rev
A3	DJ1 Calpella UMA		X01
Date:	Friday, April 16, 2010		Sheet 80 of 90

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Title Reserved			
Size C	Document Number DJ1 Calpella UMA	Rev X01	
Date: Friday, April 16, 2010		Sheet 61	of 90

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File

Reserved

Size

A2

Document Number

DJ1 Calpella UMA

Rev

X01

Date: Friday, April 16, 2010

Sheet 82 of 90

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Title Reserved		
Size C	Document Number DJ1 Calpella UMA	Rev X01
Date: Friday, April 16, 2010 Sheet 63 of 90		

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Title

Reserved

Size

Document Number

Custom

DJ1 Calpella UMA

Rev


X01

Date: Friday, April 16, 2010

Sheet 84 of 90


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Title Reserved			
Size Custom	Document Number DJ1 Calpella UMA		Rev X01
Date: Friday, April 16, 2010	Sheet	85	of 90


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Title			
Reserved			
Size	Document Number		Rev
A3	DJ1 Calpella UMA		X01
Date:	Friday, April 16, 2010		Sheet 86 of 90

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Title			
Reserved			
Size	Document Number		Rev
A3	DJ1 Calpella UMA		X01
Date:	Friday, April 16, 2010		Sheet 87 of 90


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File		
Reserved		
Size	Document Number	Rev
C	DJ1 Calpella UMA	X01
Date: Friday, April 16, 2010		
Sheet 68 of 90		

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	46	2010/04/16	Power team	PU4603 (RT8205) shortage risk	Change to TPS51125	X01
2	50	2010/04/16	Power team	PU5002 (RT8207) shortage risk	Change to TPS51116, DY PR5011	X01
3	49	2010/04/16	EE	PM_PWROK to +1.05V_VTT power down sequence out of SPEC	Modify PC4907=0.022U,PR5004, add R4905=1K	X01
4	55	2010/04/16	EE	For SIV CRT test fail item	Modify RN5504=100 Ohm	X01
5	50	2010/04/16	Power team	Cost down	DY PTC5001	X01
6	53/13	2010/04/19	Power team	Power team request	Change PC5321=0.015U, PC5326=0.01U, PR5312 Mount PC5319,PC5312,PC5311,C1325,C1328,C1323	X01
7	47/12	2010/04/19	Power team	Power team request	Modify PR4705=2,8K, PR4727=1.4K Mount C1214=C1236=C1241=C1208=C1231=10U	X01
8	79	2010/04/19	ME	For EMI	Add SPR1	X01
9	79	2010/04/21-22	EMC	For EMI	Add EC7972-EC7981(DY) Mount EC7938,EC7947,EC7954	X01
10	26/37/47/51/53/	2010/04/21	EE	Cost down	Change 0 Ohm resistance to 0 Ohm pad: R2611,R2603,L3701,PR4706,PR4708,PR4713,PR4718, PR4722,PR4732,PR4738,PR4744,PR4755,PR4764, PR4707,PR4711,PR4776,PR4784,PR4703,PR4704, PR4790,PR5102,PR5310,PR5313,PR5314,PR5317, PR5333	X01
11	60	2010/04/21	EE	for audio vender's seggust	Modify R6009,R6010 to 0 Ohm resistances	X01
12	37	2010/04/21	EE	For version ID	Mount R3722, DY R3725	X01
13	46	2010/04/22	Power team	For power snubber	Mount PR4606=PR4607=2R2, PC4620=330P, PC4621=680P	X01
14	46	2010/04/22	Power team	For OCP	Modify PR4603=140K	X01
15	47	2010/04/23	Power team	For power snubber	Modify PR4717=10K	X01



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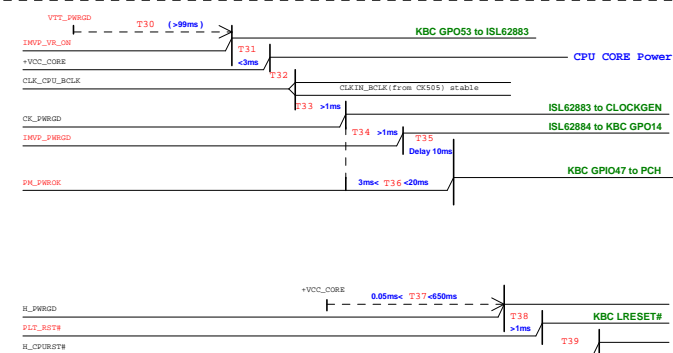
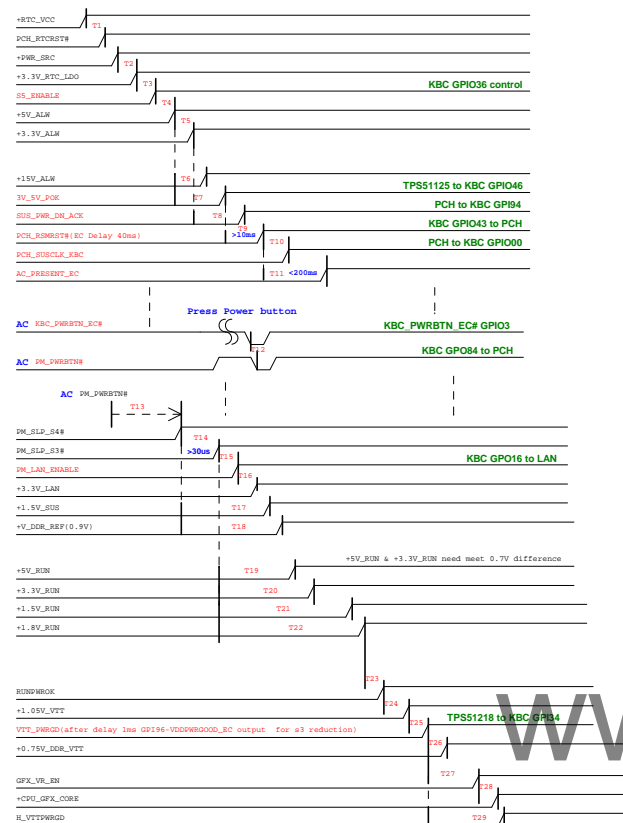
Title: **Change History**

Size A3	Document Number DJ1 Calpella UMA	Rev X01
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Date: Monday, April 26, 2010 Sheet 89 of 90

(AC mode)

red word: KBC GRIO



(DC mode)

red word: KBC GPIO

